3DS IC International Standards
SEMI 3D IC Standards Program

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Outline

• SEMATECH 3D Enablement Center
  – Developing standards
• Standards Landscape for 3D
• SEMI Standards
  – Documents
  – Experimental support
    • Precision and bias statement
• 3D Standards Wiki
3D TSV Outlook

• **Near future (2011–2013)**
  – Interposer products
  – Wide IO DRAM (mobile)
    • Performance, power, Footprint, & cost

• **Future (2013–2017)**
  – Heterogeneous integration (beyond memory on logic)
  – Higher (>5 stacking levels)
  – Smaller (<5 micron wide, >10 aspect ratio)

• **Far future (2017–2025)**
  – Beyond CMOS ( photonics, sensors, etc.)
3D Enablement Center

• Program announced December 2010 by SEMATECH, SIA, and SRC
  • Designed to meet diverse needs of SIA members: high performance, mobile, analog, mixed signal, MEMS, fabless, fablite, IDMs
  • Address gaps identified in SEMATECH industry-wide survey

  SEMATECH, SIA and SRC Team to Establish New Collaborative Program for Enabling 3D ICs
  
  Industry pulls together to develop industry standards to guide 3D integration and accelerate technology adoption

  Albany, NY and WASHINGTON (December 8, 2010) – SEMATECH, the Semiconductor Industry Association (SIA), and Semiconductor Research Corporation (SRC) announced today they have established a new 3D Enablement program to drive cohesive industry standardization efforts and technical specifications for heterogeneous 3D integration. Through the guidance of SEMATECH working in partnership with SRC, the program aims to establish the infrastructure necessary for the industry to leverage 3D packaging technology for innovative new applications.

• Mission:
  • Enable industry-wide ecosystem readiness for cost-effective TSV-based 3D stacked IC solutions

• Members:
  • **Enablement Center:** Altera, ADI, Invnesas, LSI, NIST, ON Semi, and Qualcomm
  • **3D Program:** SK hynix
  • **SEMATECH Core:** CNSE, GLOBALFOUNDRIES, IBM, Intel, Samsung, TSMC, and UMC

• New members welcome!
3D Enablement Center

• Initial focus is on wide IO DRAM for mobile applications
  • Provide clarity to help identify gaps in standards, specifications, technologies
  • Also explore high performance computing, others

• Inaugural activity
  – Industry survey
SEMATECH Survey Results
Gaps in the Via-Mid Ecosystem

• 12 companies surveyed Aug-Sep 2010: IDMs, foundries, fabless, OSATs
• High density via-mid applications including interposers, heterogeneous stacking, logic on logic, memory on memory; 2011-2014 timeframe
• Addresses all aspects of via-mid: wafer processing, assembly, reliability, inspection/metrology, design, test
• Highest priorities for heterogeneous stacking (e.g., wide IO DRAM) shown below

Gaps in Standards and Specifications
• EDA Exchange Formats
  – Partitioning and floorplanning; logic verification; power/signal integrity analysis; thermal analysis flow; stress analysis flow; physical verification; timing analysis
• Reliability
  – Reliability test methods
• Test
  – DFT test access architecture
• Inspection/metrology
  – TSV voids, defect mapping, microbump inspection and coplanarity
• Chip Interface
  – Stackable memory pin assignment; stackable memory physical pinout
• TSV
  – Keep-out area, fill materials, dimensions
• Thin wafer handling
  – Universal thin wafer carrier

Technology Development and Cost Reduction
• Reliability
  – Criteria; test methods; ESD
• Temporary bond/debond cost reduction
  – Materials and release mechanisms cost reduction; Equipment cost reduction
• TSV
  – Keep-out distance/area
• Microbumping and bonding
  – Pad metallurgy and layer thickness; bump metallurgy
• Inspection/metrology
  – Microbump inspection and coplanarity; TSV voids; BWP voids
• Test
  – Probing microbumps cost reduction
3D Enablement Center
Ongoing Activities (I)

• Develop reference flows to identify needed standards (and technologies)
• SEMI® standards and standards orchestration
  – Leadership: NIST assignee to SEMATECH co-chairing 3DS-IC NA committee, chairing BWS task force, and co-chairing Bonded Wafer Task Force in MEMS/NEMS committee
  – Providing wafers to supporting task forces
    • D5270: Guide to Measuring Voids in Bonded Wafer Stacks
    • D5175: Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers
3D Enablement Center Ongoing Activities (II)

- Development of inspection/metrology specifications
- Microbump/bond metallurgy specifications
- Near-term university research (SRC)
- Design exchange formats
- Development of an easy to use public website for standards related to 3D ICs
3D Enablement Center
Future Activities

• Future programs under consideration:
  • Pathfinding
  • EDA tools
  • Test vehicles
Reference Flows

- **Objective:** Identify and prioritize needed standards, specs, and technologies
- **Initial focus:** Mobile wide IO DRAM
- **Second focus:** High performance wide IO DRAM
- **Approach**
  - Survey member companies to define requirements
  - Compare pros and cons of various reference flow options
  - Identify needed standards, specs, and technologies

**Wide IO Performance and Size**

- Best of both worlds (Wide IO + TSV)
  - Wide IO: For performance
  - TSV: For thin multi-die stack

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1200 bumps, 40x50 µm pitch
## Comparison of Mobile and High Performance Wide IO Applications

<table>
<thead>
<tr>
<th>Structure Limitation</th>
<th>Computing Wide IO (High Performance)</th>
<th>Mobile Wide IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>Dependent on design, technology, and cooling technique</td>
<td>Serious</td>
</tr>
<tr>
<td>Data Band Width (Speed)</td>
<td>( \leq 64 \text{ GB/s} )</td>
<td>( \leq 12.8 \text{ GB/s} )</td>
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<tr>
<td>Power</td>
<td>10-150W</td>
<td>2-20W</td>
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<tr>
<td>Interposer</td>
<td>Can be used</td>
<td>Not Used</td>
</tr>
<tr>
<td>Structure for Thermal</td>
<td>Use heat sink and TIM</td>
<td>-</td>
</tr>
<tr>
<td>Structure</td>
<td><img src="image1.png" alt="Diagram 1" /></td>
<td><img src="image2.png" alt="Diagram 2" /></td>
</tr>
</tbody>
</table>
Mobile Wide IO Reference Flow

- Case 1: Logic TSV (DtS) => Memory cube to Logic TSV (DtD) => Backend (molding/BA/singulation)

- Case 2: Logic TSV to Memory cube (DtD) => Memory cube + Logic to sub => Backend (molding/BA/singulation)
SEMATECH 3D Enablement Center

» Overview of Activities

3DS Standards and Reference Flow

3D Wiki Site

» Wiki Site Demonstration
SEMI® 3D Standards Activities

MEMS/NEMS Committee
- 8 Published Standards

Current Activities
- 3 New Standards
- 4 Revisions

MEMS/NEMS Committee

3DS-IC Committee

Wafer Bond TF

- MS1-0307: Guide to Specifying Wafer-Wafer Bonding Alignment Targets (Re-approved April 2012)
- MS5-1211: Test Method For Wafer Bond Strength Measurements Using Micro-Chevron Test Structures (Updated version published Dec 2011)
3D Stacked IC SEMI Standards Approaches

- Guides
- Supporting experiments
  - Experience to provide guidance to users of the standard
  - Provide precision and bias statements
Consortia Landscape Across 3D Flow

3D Stack Planning

- GSA
- imec
- Physical Planning
- Package Planning
- Design Standards

Partitioning

Tier Design/Manufacturing

- Industry Focus/Interest Group
- 3D PDK
- Design Standards

3rd Party Tier IP

Design Standards

Standards

Research

Standards

Research

Research

Standards

Standards

Standards

IEEE Standard

Packaging & Test

Slide Courtesy of Sumit DasGupta, Si2
Required Design Flow Standards For 3D Top Level

Slide Courtesy of Sumit DasGupta, Si2
3D Design Flow Standards

3D Stack Planning
- Architecture Planning
- Physical Planning
- Package Planning

Partitioning

Tier Design/Manufacturing
- 3D PDK
- Electrical Design/Verif
- Physical Design/Verif
- Thermal/Mech Analysis
- Chip Finishing, Extraction, DRC, LVS
- Mask Creation, DFM, Data Prep
- Foundry

Multi-tier thermal estimation
Multi-tier power networks
Multi-tier parasitic networks

3rd Party Tier IP
- TSV, interposer properties
- RDL models, RDL layers, u-bumps

Partitioning and floorplanning constraints

TSV, interposer properties
API between EDA, T/M tools

Thermo-mech corner conditions

Packaging & Test

Slide Courtesy of Sumit DasGupta, Si2
Standards & 3D Reference Flow

Need to start with the elements

Logic die (C4 bump face down) → C4 process for Tier 1 → Tier 2 die to tier 1 die attach process → Molding, etc.
Standards & 3D Reference Flow

JEDEC JC-11: Wide IO Mobile Memory Mechanical Outlines

JC-42: Wide IO DRAM Memory Specification – Low Power DRAM

Si2: Open3D Technical Advisory Board (TAB)
   Develop standards to
   • Define the necessary formats/interfaces/APIs to enable
     the transfer and sharing of design and model data
     throughout 3D IC design flows
   • Enable the transfer of required design data from the 3D
     IC design system to package design systems for the
     design of packages for the 3D ICs
Standards & 3D Reference Flow

- SEMI D5268: Guide for Terminology for Measured Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures
- SEMI D5410: Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures
  * Supporting Experiment
Standards & 3D Reference Flow

 Memory Cube

 SEMI MS1-0307: Guide to Specifying Wafer-Wafer Bonding Alignment Targets

 Logic Chip
Standards & 3D Reference Flow

SEMI D5270: Guide to Measuring Voids in Bonded Wafer Stacks
* Supporting Experiment

SEMI D5409: Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks
* Supporting Experiment

SEMI MS5-0310: Test Method For Wafer Bond Strength Measurements Using Micro-Chevron Test Structures
* Completed Experiment – published with “Precision and Bias” statement
MS5 – Revision History

• First version balloted and published as MS5-1107 without supporting experiment
• Round-Robin run 2008–2010
  – Details on next slide
• Major revision, including “Precision and Bias” statement published as MS5-0310
• …and since standards work is never truly complete, minor revision published as MS5-1211
MS5 Supporting Experiment
“Round-Robin” Experiment

- Seven participating laboratories
- Samples provided by one of the laboratories
- Not a “classic” Round-Robin, since the samples are destroyed during testing
  - Following test and data analysis procedure specified in ASTM E691 — Standard Practice for Conducting an Interlaboratory Study to Determine the Precision of a Test Method
- Beta test
  - Performed using MS5-1107 version of standard
  - User identified several areas where instructions were incomplete, misleading, or misordered
  - Team rewrote Section 10, Procedure, based on beta lab experience
- Acceptable results obtained from six laboratories
Standards & 3D Reference Flow

SEMI D5173: Guide for Describing Materials Properties and Test Methods for a 300 mm 3DS-IC Wafer Stack

SEMI D5174: Specification for Identification and Marking for Bonded Wafer Stacks
* Possibility of Supporting Experiment
Standards & 3D Reference Flow

SEMI D5175: Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers
* Supporting Experiment
D5175 – History

• SNARF approved by 3DS-IC Committee in March 2011
• Writing begun in Summer 2011/Fall 2011
• Supporting experiment begun in Summer 2011
  – Purpose of experiment
    • Provide users of the anticipated standard with the tools for determining whether a particular shipping method will suit their requirements
    • Baseline test of several different shipping configurations
  – Issues identified
    • Measurement of shock experienced by wafers
    • Need for modeling
D5173 – Supporting Experiment

- Identify possible methods of shipping thin, silicon wafers
  - Multiple options and multiple vendors
- Acquire necessary thin wafers
  - Unpatterned 100 µm and 50 µm silicon wafers on dicing tape, mounted on dicing frames (SEMI G74 and G87 standard)
- Drop tests following ISO 2248:1985

- This experiment is currently in progress
Standards & 3D Reference Flow

IEEE P1838: Test Access Architecture for Stacked 3D-ICs
Points for Testing Pre- and Post-bonding

JEDEC JC-14: 3D-ICs Packaged and Unpackaged
Evaluations and Qualifications (qualification and evaluation
test methods)

JC-42: 3D Memory Stack for DDR3 and DDR4 using TSV

JC-63: 3D Stacked Mixed Technology
Standards & 3D Reference Flow

Logic die (C4 bump face down) → C4 process for Tier 1 → Tier 2 die to tier 1 die attach process → Molding, etc.
Standards & 3D Reference Flow

D5270: Guide to Measuring Voids in Bonded Wafer Stacks
MS1-0307: Guide to Specifying Wafer-Wafer Bonding Alignment Targets
IEEE P1838: Test Access Architecture for Stacked 3D-ICs
Points for Testing Pre- and Post-bonding
MS5-0310: Test Method For Wafer Bond Strength Measurements Using Micro-Chevron Test Structures

Tier 2 die to tier 1 die attach process
Molding, etc.

Logic die (C4 bump face down)
C4 process for Tier 1
Standards & 3D Reference Flow

JEDEC JC-14: 3DS-ICs Reliability Test Methods

JEDEC JEP158: 3D CHIP STACK WITH THROUGH-SILICON VIAS (TSVS): Identifying, Evaluating and Understanding Reliability Interactions

JEDEC JC-14: 3D-ICs Packaged and Unpackaged Evaluations and Qualifications (qualification and evaluation test methods)

JEDEC JC-40: 3D Stack Buffer/Register Support

JEDEC JC-42: General Memories and TSVs
SEMATECH 3D Enablement Center
» Overview of Activities

3D Standards and Reference Flow

3D Wiki Site
» Wiki Site Demonstration
3D IC Standards Landscape ("dashboard") Objectives

• Develop an easy to use public website for standards related to 3D ICs:
  – Define, track, get status, find milestones
  – Identify risk areas
  – Determine gaps related to all necessary 3D IC standards

• Provide a single monitor/coordinator function
  – To accelerate the development and adoption of standards
  – To promote the optimal use of resources
  – To avoid confusion

• Domains
  – Design exchange formats, test, design, verification, process, handling, metrology, reliability, materials
Dashboard Release

- Announcement to Working Group
  - June 22, 2011

- Public Announcements
  - July 12, 2011: SEMI 3DS-IC Committee meeting
  - July 12, 2011: SEMI Standards 3D Workshop
  - September 23, 2011: 3D-Test Workshop
Welcome to the:

3D Interconnect Wiki

3D integration holds tremendous promise for future integrated circuits. The clear advantages of 3D integration include higher performance, lower power and increased functionality in a smaller form factor. This potential is drawing considerable attention from a wide variety of companies across the semiconductor and MEMS industries.

Through-silicon vias (TSVs) are already in production for CMOS image sensors. High-volume manufacturing for Wide I/O Dynamic Random Access Memory (DRAM) utilizing TSV technology is expected as early as 2013.

The purpose of this wiki is to provide an open forum to discuss the issues which must be resolved before high-volume implementation of 3D integrated circuits becomes a reality.

We welcome your comments and inputs on these topics related to 3D integration as well as any suggestions for directions for new discussions on this Wiki.
Welcome to the:

3D Interconnect Wiki: Standards for 3DS-ICs

Despite its high potential, a lack of uniform standards have slowed the migration of 3D technologies into mainstream production. In particular, cost-effective high-volume 3D integration of ICs from multiple sources will require the development of a cohesive set of end-to-end standards at the interfaces between supply chain partners.
The main objective of the 3D-ICs Standard Activities Dashboard is to have a public and centralized website to provide easy to use links to the standard development organizations (SDOs) involved in standards development for 3D-ICs. This site will allow the 3D-IC community to define, track, provide status, find milestones, identify risk areas, and to determine gaps related to all necessary standards for the development, design, process, manufacturing, verification, and test of 3D-ICs and associated package technologies.

We welcome your comments and participation on this wiki. We especially seek the 3D-IC community’s help in identifying standards development activities that have not yet been captured on this dashboard. In addition, we seek to use this site to identify areas where standards are needed. You may put your suggestions as comments to these pages or send an email to Rich Allen at SEMATECH.

If you would like to comment, we do ask that you register following the link below and use your first and last name.

The community has, to date, identified standard relevant to 3D Stacked ICs from the following SDOs:

- **3D-IC Alliance**
- **IEEE**
- **JEDEC**
- **SEMI**
- **SI2**

**Comments (0)**
# 3D Standards Dashboard

## Published Standards (Click on each Standard for direct access from SDQ)

<table>
<thead>
<tr>
<th>Domain</th>
<th>Standard</th>
<th>Organization</th>
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<tbody>
<tr>
<td>Memory Interface</td>
<td>IMMI™ - Interfacing Memory Interface Specification</td>
<td>JEDEC</td>
<td>Published Standard</td>
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<tr>
<td>Guide</td>
<td>JEP108: 3D Die Stack Reliability Handbook</td>
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<td>Published Standard</td>
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## Standards Activities in Progress

| Testing DFT/MTPG | Test Access Architecture for 3D Stacked I/Os and DFT, Wafer Probe Interface, Board-Level Interconnect Test, Board-Level Access to Embedded Instruments | IEEE          | Organization/On target |

## Glossary

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<th>Term</th>
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## 3D Standards Dashboard

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<td>Memory - Wide I/O DRAM</td>
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<td>JEDEC168: 3D DfM Study Reliability Inclusion</td>
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<td>Metabase</td>
<td>JEDEC-0011: Test Method for Wafer Bond Strength Measurements Using Nickel/Gold Metalization</td>
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### Active Technical Standards Ballot

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### Standards Activities in Progress

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SEMI Downloads

SEMIMS51211 - Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures

Language: English

Volumes(s): MEMS

Status
CURRENT - Supported by the technical committee.

Add to Cart
$100.00

Abstract

This Standard was technically approved by the global MEMS/MEMS Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on September 12, 2011. Available at www.semiviews.org and www.semi.org in December 2011; originally published November 2007; previously published March 2006.

This Test Method enables the determination of the bond strength between two wafers using micro-chevron test structures. Wafer-wafer bonding is a mainstay for microelectromechanical system (MEMS) and three dimensional stacked integrated circuits (3D-SiP) design and fabrication. MEMS components, such as acceleration sensors, gyroscopes, micro-pumps, or microvalves that are increasingly found in smart automotive and navigation control systems or in medical devices typically use wafer bonding technologies. Due to being subjected to mechanical stresses, the industrial applications of these components require high mechanical strength, low leakage, and high reliability of the wafer-bonded interface. For a knowledge of the strength determining factors (such as fatigue and stress corrosion) of wafer bonding, for quality control, and for the development of new bonding technologies, a method for determining the strength of such bonds is important to producers and users of MEMS devices, of wafer bonding equipment, and of wafer materials.
The main objective of the 3DS-ICs Standard Activities Dashboard is to have a public and centralized website to provide easy to use links to the standard development organizations (SDOs) involved in standards development for 3DS-ICs. We welcome your comments and participation on this dashboard. We especially seek the 3DS-IC community’s help in identifying standards development activities that have not yet been captured on this dashboard. In addition, we seek to use this site to identify areas where standards are needed. You may put your suggestions as comments to these pages or send an email to Rich Allen at SEMATECH.

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Return to Standards for 3DS-ICs
Do You Agree to the Terms?

By registering on this website you accept, without limitation or qualification, all of the guidelines and terms of use.

Registering grants permissions to comment on pages. If you wish to contribute content to the wiki, please see the Contributors page.

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Password: 
Confirm Password: 
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Time Zone: Site Default (US/Eastern) ▼
The site will adjust times displayed on the site to your location.

Signature: clarkm
Type the two words: [Captcha]

Register  Cancel
Commenting on 3D Standards Dashboard

Submitted By: Rich Allen

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<tr>
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<td>Metrolgy</td>
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### Standards Activities in Progress

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<td>Test Access Architecture for 3D Stacked ICs and DFT, Wafer Probe Interface, Board-level Interconnect Test, Board-level Access to Embedded Instruments (F-1833)</td>
<td>IEEE</td>
<td>Organization</td>
</tr>
</tbody>
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SEMATECH

SEMI Standard Activities

Introduction
Semiconductor Equipment and Materials International (SEMI) is the global industry association serving the manufacturing supply chain for the micro- and nano-electronics industries. One of its key services is the SEMI International Standards Programs, which produces standards in areas including materials, processes, and safety for the semiconductor, photovoltaic, and flat panel display industries.

List of Standard Activities/Listed by Committee and Task Force

NA 3DS-IC Committee

- 3DS-IC Bonded Wafer Stacks (WSB) Task Force
  - Guide for Describing Materials Properties and Test Methods for a 300 mm 3DS-IC Water Stack (DS175)
  - Specification for Identifying and Characterizing the Quality of Wafer Stacks (DS174)

- 3DS-IC Inspection and Metrology (IBM) Task Force
  - Guide for Terminology for Measured Geometrical Parameters of TSVs in 3DS-ICs (DS209)
  - Guide for Detection and Characterization of Voids (DS270)
  - Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bump, Wafer/SiP, and Flatness of Bonded Wafer Stacks (DS409)
  - Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures (DS410)

About this Wiki
The purpose of this Wiki is to provide a forum to discuss the challenges, and...
Rationale: Current wafer standards (SEMI M1) do not adequately address the needs of wafers used in bonded wafer stacks. Wafer thickness, edge bevel, notch, mass, bow/warp and diameters are changed when wafer stacks are bonded together, or wafer stacks bonded and thinned. These deviations from wafer parameters specified in SEMI M1 have numerous impacts in other equipment and hardware standards that reference SEMI M1, and SEMI drives a new standard to reflect wafer parameters associated with bonded and bonded/thinned wafer stacks.

This document was recently balloted. At the SEMI Spring meetings, the JCCS-IC Committee found the Negative votes to be 'Technically Relevant and Persuasive' and sent the document back to the Bonded Wafer Stack TF to revise and prepare for re-ballot in Cycle 4, 2012 (May). This revision in currently in progress - please contact us at the link below if you are interested in helping modify this document for re-ballot.

Organization: SEMI
Domains: Mfg/Process
Activity Type: New Standard/Document (5173)
Committee: JCCS-IC
Task Force: Bonded Wafer Stacks (BWS)

Links:
Organizing Document
Ongoing Activities

Key Contact: Richard Allen
Standards Dashboard

• One-stop location to identify ongoing standards activities
  – 3D standards activities are currently spread across a wide range of SDOs

• Open for public access and comment
  – Open dialog among members of the standards community
  – Help identify unmet standards needs
  – Encourage participation in standards
A Wiki’s value is its community…
Please join our conversation at

[wiki.sematech.org](http://wiki.sematech.org)
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