Innovative Advanced Wafer Level Packaging with Smart Manufacturing Solutions

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Outline

1. Introduction of Smart Manufacturing & Wafer Level Packaging

2. Smart Manufacturing in Wafer Level Packaging

3. Scalability - Panel Level Fan Out Wafer Level Packaging

4. Summary
SMART Manufacturing Elements

- Information
- Smart Control
- Smart Sensors
- Visualization
- Safety
- Network and Security
Wafer Level Packaging
(200/300mm)
Wafer Level Packaging Process

- No Wirebonding
- No Flipchip
- No Substrate/Leadframe

- Wafer Level Process
- Fab-like process with SOD coating, Mask aligner/stepper, plasma, Sing wafer etching
- Highly used for mobile products; RF, PMIC, connectivity, Analog, MCU, etc.

- **Smallest and Thinnest PKG solution ever after**
- But limited due to its PKG size equal die size
Typical Wafer Level Packaging Process
Assembly Factory Planner

[STEP 1] Target Generation
- Step targets (In/out)
- WIP progress for each demand
- Latest process start time (LPST) by lot

[STEP 2] Capacity Planning
- Estimated step completion times
- Machine schedules
- Assembly out

Planning Engine:
- Demand (MP)

Backward Planning Simulation

Constraints & Rules:
- Cycle-time/Yield per Step
- Demand/WIP priority
- Product branch & site allocation
- Processing constraints

Forward Planning Simulation
- EQP arrange (dedication)
- EQP-step flow time & tact time
- Dispatching rules / job change rules
- PM (preventive maintenance) schedule

In/out Plans & Schedules
In order to enhance an OSAT’s competitive power on *pricing*, its *line operation management system (OMS)* should be able to

1) Minimize WIP to reduce *turnaround time (TAT)* and avoid deterioration defects

2) *Increase the number of tools per worker* to reduce TAT and labour costs

3) *Maximize resource utilization*;

4) *Increase global efficiency of the IC chip supply chain*
The OMS for OSAT manufacturing should be capable of:

- Increasing the number of tools per worker for TAT reduction
- Enhancing the visibility of the supply chain
- Providing reliable RTF values
- Minimizing WIP
- Maximizing resource utilization
- Increasing the global efficiency of the IC chip supply chain
Process Management System

- Alternative production line scenarios (Mixed model line balancing)
- Making assembly lines more efficient with reduced lead time
- Shorter product times and reduced work in progress (WIP) inventories
- Allowing rapid response to product or product changes.
- DFM (Design for Manufacturing)
## Yield Management System

- As the need for more data relevant to making improvements in manufacturing yields becomes more acute due to the tremendous leverage of yield on manufacturing costs.
- The extremely large amount of data now available for this purpose needs to be managed in a systematic way to ensure the efficient implementation of improvement programs.

<table>
<thead>
<tr>
<th>Fab Lot ID</th>
<th>Yield Breakdown (%)</th>
<th>Overall Assembly Yield (%)</th>
<th>PKG O/S Defect From Final Test</th>
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<tr>
<td>Lot #1</td>
<td>99.98 99.66 99.88</td>
<td>99.52</td>
<td>0.03%</td>
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<tr>
<td>Lot #2</td>
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<tr>
<td>Lot #3</td>
<td>99.96 99.86 99.89</td>
<td>99.71</td>
<td>0.03%</td>
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FO WLP – Large Panel Size with Cost Effectiveness
Wafer Level Package Expansion to Fan-Out

- FOWLP is a new Wafer Level Packaging technology, utilizing well developed wafer bumping infrastructure, with an innovative wafer reconstitution process to package Known Good Dice.

- Wafer level package, uses mold compound to support the fan-out I/Os.

Fan-In WLP
PKG size = Chip size

Fan-Out WLP
PKG size > Chip size

- Fan-In Interconnects only - Number and pitch of Interconnects must be adapted to the chip size
- Only Single chip packaging solution

- Fan-out Interconnects - #, Pitch of Interconnect is INDEPENDENT of chip size
- Single/Multi/3D chip packaging solution
- Improved Yield with KGD

FOWLP expands the application space for Wafer Level Packaging!
High Performance Solution with Increased I/O Density

- Thinner and Smaller Form Factor
- Enhanced Performances
- Integration — multi-Die, 3D PoP & SiP
- Cost Effective Solution with Scalability
- Manufacturing proven Solutions (HVM from 2009)

Integration with multi-die, embedded discrete and RDL inductor

Ultra Thin PKG ~0.3mm with solder ball

Fine Cu Plated RDL 5/5um → 2/2um LW/LS

Ultra Thin eWLB 10mm
FO WLP Process Flow

1. Reconstitution of dies to "artificial" panel
   - Single die or several (different) dies, actives and passives
   - Molded artificial wafer is starting point for thin film technology

2. Redistribution
   - Using thin-film-technologies
   - Using standard thin-film equipment
   - Using commercially available materials

3. Ball Apply and Singulation
   - Standard backend assembly flow (and equipment)

4. Test, Mark, Scan, Pack
   - Standard or wafer level based test flow
   - Standard assembly

eWLB FOWLP schematic
• Higher integration capability with FO-WLP will give access to markets where nowadays FCBGA PoP/SiP are dominating.

• FO-WLP starts to appear in some complex applications: PMIC, RF, GPS, Wifi, Audio Codec and some specific niche applications in space and medical.

• Yole projections show 32% CAGR for non-Apple/TSMC revenue through 2020

• SCL internal projections indicate even higher growth is possible (OSAT industry capacity limited)
**FlexLine™:** A Flexible Wafer Level Packaging Manufacturing Solution

*FlexLine™ process flow dices incoming wafers at the start of the process, enabling reconstitution into an optimized panel size.*

- FlexLine™ provides a [Simplified Supply Chain](#)
- One qualified manufacturing source can provide FI-WLP, eWLCSP, FO-WLP, 2.5D eWLB, and 3D eWLB using the same [Simplified of Bill of Materials (BOM)](#)
- Maximizes flexibility with current equipment set
- FlexLine™ enables a durable and [lower cost WLCSP](#) supply chain option for various wafer sizes (150, 200, 300mm) today

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[Diagram: A Single Manufacturing Module with Optimized Panel Size]

**eWLB/ eWLCSP**
FOWLP  Cost Structure

- FOWLP process has numerous steps that can be divided into major cost blocks
  - Front End Assembly Processes (Cost is nominally die size dependent)
    - Incoming wafer prep, mount, saw, and panel reconstitution
  - RDL (Cost is dependent on die area on panel)
    - Panel based process to apply redistribution layers on panel
  - Back End Assembly and Singulation Processes (Cost is die size dependent)
    - Laser mark, AOI, Carrier Saw, PKG Pick-n-Place
  - Cost contribution of the major areas is shown below.

- Cost varies based on body size.
- *The variation in carrier cost creates a large percentage unit cost difference.*
- Body size impacts overall cost and should be optimized for the lowest cost solution.
FOWLP Move to Larger Scale

- 12”x12” square panel area is increased more than 30% compared to a 12” wafer because the square panel saves corner space.
- Significant cost and productivity advantages can be achieved with the larger scale reconstituted wafer eWLB format due to higher efficiency and economies of scale.

Circle

100

> 30% + Units Increase

Square

~130

600x600mm Panel = 6.5x
500x500mm Panel = 4.54x
300x300mm Panel = 1.64x
300mm Dia = 1x
Economies of scale arise when the cost per unit falls as output increases. Economies of scale are the main advantage of increasing the scale of production and becoming ‘big’.

i) Firstly, because a large business can pass on lower costs to customers through lower prices and increase its share of a market.

ii) Secondly, a business could choose to maintain its current price for its product and accept higher profit margins.
Cost Scaling with Larger Carrier Sizes

- FOWLP manufacturing lends itself to the use of larger carrier formats which has a direct impact on capital intensity and cost
- HD carrier formats have been qualified in volume production line since 2015
- Panel level processing is the most sensible for larger body sizes above 10x10mm
Challenges of Panel FOWLP

• Warpage Control
  – Heterogeneous materials and nonsymmetric Structures can cause bowing & distorsion
  – EMC, Dielectric polymer materials with adapted CTE and modulus, plus shrinkage control

• Process control and Manufacturing – new approach with panel size
  – Innovative processes for high volume manufacturing
  – Improved optical recognition systems for placement equipment & inspection tools
  – Imaging solutions with high depth of focus and high resolution

• Yield Control and Cost Effectiveness
  – Suited materials (BOM) with design for reliability & manufacturing
  – Optimized processes with simple steps
  – Available Equipments compatible to panel process
Challenges of Panel FOWLP

Panel Manufacturing Experience
- Printed Circuit Board (PCB)
- Display (LCD, OLED) technology
- Solar Cell Panel
Summary

• Smart Manufacturing – Innovation & Value-Up through Big Data and IoT Integration
• Wafer level packaging - Wafer fab friendly assembly technology, expanding to FO WLP
• Panel Level FO WLP – Scalability with larger panel size for lower cost solution,
• Challenges and Opportunity for Panel Level FO WLP - panel handling capability