Packaging Wars Begin

OSATs and foundries begin to ramp offerings and investments in preparation for mainstream multi-chip architectures.

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The advanced IC-packaging market is turning into a high-stakes competitive battleground, as vendors ramp up the next wave of 2.5D/3D technologies, high-density fan-out packages and others.

At one time, the outsourced semiconductor assembly and test (Outsourced Semiconductor Assembly and Test) vendors dominated and handled the chip-packaging requirements for customers. The landscape began changing several years ago when TSMC entered the advanced packaging market. Since then, two other foundry vendors—Intel and now Samsung—announced plans to enter the advanced packaging business. The moves put the three foundry vendors in direct competition with the OSATs, although not all foundries are competing against the packaging houses.

Still, some foundries are taking a significant bite out of the business. For the new iPhone7, TSMC is making the A10 application processor on a foundry basis for Apple, according to Yole Développement. Based on a 16nm finFET process, Apple’s A10 is housed in TSMC’s Integrated Fan-Out (InFO) technology, the research house said.

Now, TSMC is developing a second-generation fan-out package and is spending roughly $1 billion in advanced packaging. And Intel said that its R&D spending in packaging is more than the two largest OSATs combined.

In response to the foundries and other events, several OSATs are consolidating as part of an effort to combine their resources and R&D. For example, Advanced Semiconductor Engineering (ASE), the world’s largest OSAT, plans to merge with one large rival and is investing in another.

But the changing landscape will present some challenges for customers. First, many chipmakers and OEMs are still evaluating various next-generation package types for their future products. Finding the right solution is complex and difficult.

In addition, customers must select a vendor for their advanced packaging requirements. Customers could go one of following routes:

• A turnkey service from a foundry. This involves everything from front-end manufacturing to IC-packaging and test.
• An OSAT.
• A combination of both foundries and OSATs.

So what’s the best path? The answer depends on the requirements. Each route has some advantages and disadvantages. For example, in the turnkey approach, the foundry manages the supply chain and production flow, thereby controlling the cost and yield for customers. But the turnkey approach is less flexible and usually prevents customers from working with their preferred OSAT partners.

Ultimately, the decision comes down to several factors. “The market is going to determine who does it,” said Jim Walker, an analyst with Gartner. “It’s all based on cost.”

There are other considerations. At last count, for example, a dozen or so companies are developing fan-out packages, but it’s unclear if all vendors or technologies will succeed in the long run. “Since
this is an emerging market, there is enough room for all of them until the market matures,” Walker said.

**What is advanced packaging?**

A number of OSATs and foundries are pursuing advanced packaging for good reason—it’s a hot market. In fact, some foundries are looking for new growth engines amid a slowdown in the IC industry, and packaging presents some new and sizeable opportunities.

In total, the advanced packaging market is expected to reach $30 billion by 2020, up from $20.2 billion in 2014, according to Yole. Flip-chip is still the largest market in this area, but fan-out is growing the fastest. In total, the fan-out packaging market is projected grow from $244 million in 2015 to $2.4 billion by 2020, according to Yole.

Meanwhile, the separate market for 2.5D technology using **through-silicon vias (TSVs)** is expected to grow at an annual rate of 22% from 2014 to 2020, according to the firm.

Momentum is building for advanced packaging for several reasons. In simple terms, chipmakers want smaller packages with more performance. “Nowadays, there are several considerations on how you implement the chip,” said Walter Ng, vice president of business management at UMC. “Packaging is as much an upfront decision as anything else. It can certainly impact overall cost and performance.”

For example, smartphones have traditionally incorporated a packaging technology called **package-on-package (PoP)**. This utilizes flip-chip interconnects in a ball grid array (BGA) package. PoP stacks two or more separate dies on top of each other. A memory package is on the top, while an application processor or baseband die is on the bottom.

PoP is still used in smartphones, but the technology is running out of steam at thicknesses of 0.5mm to 0.4mm. “(POP) also starts to show some limitations in terms of bandwidth and power,” said Doug Yu, senior director of integrated interconnect and package technology at TSMC.

Seeking to displace today’s PoP packages, OSATs and several foundries have been working on an array of new and competitive technologies.

One of those technologies is called **fan-out wafer-level packaging**. Wafer-level packaging involves packaging an IC while it’s still on the wafer, enabling smaller packages.

Wafer-level packaging involves two basic technologies—chip-scale packaging (CSP) and fan-out. CSP is a fan-in technology, where the I/Os are situated over the solder balls in the package. Fan-in runs out of steam at about 200 I/Os and 0.6mm profiles.

In fan-out, individual dies are embedded in an epoxy material. The interconnects, according to Deca Technologies, “are ‘fanned out’ through a redistribution layer (RDL) to the solder bumps,” enabling more I/Os.

“We see market opportunities for (fan-out) going from small low pin count applications all the way through to very high pin count devices such as FPGAs,” said Garry Pycroft, vice president of sales and marketing for fan-out packaging specialist Deca. “We also see many opportunities for multi-chip solutions, notably as companies look to partition their analog and digital blocks of their SoCs in different fab technologies to gain the most effective option.”

Indeed, fan-out provides customers with several options. For example, it enables a multi-die package with leading- and/or trailing-edge chips.

Or, instead of moving down the traditional scaling path with system-on-a-chip (SoC) designs, fan-out also enables highly-integrated, system-level packages with existing chips. “This is definitely a consideration, as SoC integration has too much NRE cost and a slower-time-to-market,” Gartner’s Walker said. “(Fan-out has) the ability to meet various volume demands for many IoT applications.”
Still, customers face some complex choices. Basically, there are three main types of high-density, fan-out technologies—chip-first/face-down; chip-first/face-up; and chip-last, sometimes known as RDL first.

“Chip first is a process whereby the die is attached to a temporary or permanent material structure prior to creating the RDL, which will extend from the die to the BGA/LGA interface,” said Ron Huemoeller, vice president of worldwide R&D at Amkor. “The reverse is true for a chip last process. The RDL is created first and the die is then mounted.”

The first wave of fan-out packages, called embedded wafer-level ball-grid array (eWLB), were chip-first/face-down. Generally, these are lower-density packages at 10u line/space.

Source: STATSchipPAC.

Today, ASE, JCET/STATS, Namium and others are pursuing second-generation fan-out packages based on the chip-first/face-down approach. This technology, also called eWLB, is used for finer-pitch packages. It is ideal for smaller die sizes, lower I/Os and a fewer number of RDLs.

Meanwhile, TSMC and Deca are separately pursuing the chip-first/face-up approach. TSMC’s chip-first technology supports more I/Os, 3-plus RDL layers, and 2μ line/space.

Amkor is pursuing the chip-down approach. “It is used for application processors in combination with memory and other die,” Huemoeller said. “It deploys 3-plus layers of RDL and up to a 20mm square body size.”

Today, Apple is one of the first customers using high-density fan-out, but many other OEMs are taking a wait-and-see approach as the technology is still relatively expensive. “The traditional eWLB-type fan-out is cost-effective enough for even the second tier OEMs,” Huemoeller said. “The second-tier (OEMs) are willing to pay a slight premium to access the advanced technologies if the performance gain is big enough. However, it can only be a slight premium over standard product technologies.”

There are other issues. For example, OEMs want a second-source for a given fan-out package. The problem is there are no standards for fan-out, so OEMs must deal with proprietary solutions from vendors.
Besides fan-out, the market is heating up in other high-end packaging markets. In this segment, there is 2.5D stack die using interposers and TSVs. So far, the technology is gaining traction in FPGAs, graphics chips and memory.

In addition, Intel is pushing a technology called Embedded Multi-die Interconnect Bridge (EMIB). “The real key advantage of EMIB is that it requires only tiny pieces of silicon at the die borders to connect together the silicon in the package,” said Mark Bohr, senior fellow and director of process architecture and integration at Intel. “Compare this to an interposer in 2.5D. You’ve got one huge piece of silicon, which is much more expensive.”

**Going with a foundry**

Selecting the right technology is only part of the challenge. Vendor selection is also difficult, especially when choosing between a foundry or an OSAT.

Generally, there are two types of foundries in this arena. The first type doesn’t compete in the packaging market and works with OSATs. But many these foundries also provide limited packaging production capabilities, such as interposer development and TSV formation.

The second type of foundry develops and sells its own package types and may provide a turnkey service. They will also work with OSATs, depending on the product type.

The full-service foundry provides an impressive list of offerings, but they also operate at a different cost structure than the OSATs. “The foundry guys are used to doing 40% to 45%, upwards to 50% gross margins,” Gartner’s Walker said. “The packaging guys are used to doing about 20% to 25%. (The foundries) have to be willing to accept less margin to do the same process steps as the packaging guys do.”

Still, the foundries can offset some of the costs in packaging. By providing front-end manufacturing services, they can absorb some of the margin at the backend.

There are other tradeoffs. “For the most part, the foundry guys are sole-sourced when you use them,” Walker said. In contrast, a chipmaker tends to use two or three OSATs for a given package.

Meanwhile, each foundry vendor has a different strategy. For example, TSMC provides a turnkey service for its 2.5D and fan-out packages. In doing so, the company provides customers with a total solution, according to TSMC’s Yu.

Intel, meanwhile, also provides a turnkey service, although it will work with OSATs. “We don’t put any artificial constraints on the business,” said Zane Ball, vice president in the Technology and Manufacturing Group at Intel and co-general manager of Intel Custom Foundry. “Typically, once customers see what our assembly and test capabilities are, that tends to be a highlight of the collaboration.”

Another foundry, Samsung, has a different strategy. “We are not isolating the OSATs,” said Kelvin Low, senior director of foundry marketing at Samsung. “We don’t think that is a good idea. We think having a healthy ecosystem around the foundry business is still important.”

Samsung recently opened up its internal packaging and substrate operations for customers. Today, the company offers 2.5D technologies, fan-out and other packages.

Like Intel and TSMC, Samsung provides a turnkey service. “We have customers that want that,” Low said. “For us, it’s more like being a coordinator. How we consign the service is up to us.”

In many cases, though, Samsung will initiate the discussions with customers on packaging and may even ramp up a package to a limited degree. But for the most part, Samsung wants to avoid the high-volume packaging game. It prefers to offload the high-volume business to the OSATs.
“We have not changed our strategy here. Working with ASE, Amkor and others is important,” Low said. “It’s hard for us to manufacture everything. It’s not practical.”

Still others have different strategies. For example, Micron sells a 3D DRAM product called the Hybrid Memory Cube (HMC). As part of the flow, GlobalFoundries handles the TSV formation process and other steps for Micron’s HMC.

GlobalFoundries also develops interposers on an R&D basis, but it doesn’t develop chip packages for the commercial market—nor does it want to compete against the OSATs. “We work with the OSATs,” said Gary Patton, chief technology officer at GlobalFoundries.

Meanwhile, UMC provides front-end TSV manufacturing services, but it is staying out of the packaging business and works with OSATs. “Large and smaller companies generally want flexibility,” UMC’s Ng said. “They want the flexibility to choose the solution. They don’t want to be told: ‘This is the solution and take it or leave it.’ So our strategy is to continue to work with the ecosystem partners. We want to try to support those companies. We don’t want to put them out of business.”

**Working with OSATs**

Like the foundries, the OSATs have some advantages and disadvantages in advanced packaging. OSATs may have some but not all of the technical capabilities in the arena. But unlike the foundries, OSATs are more flexible and can handle large product mixes. “OSATs are built to handle product shifts, reuse of equipment and market re-direction,” Amkor’s Huemoeller said. “(OSATs have the) ability to receive die from multiple foundries to produce the final package. This is critical for SiP packages.”

Still, customers must keep a close eye on the OSATs. Over time, fewer OSATs can afford to make the necessary investments for both mainstream and advanced packages. There is only a finite amount of R&D dollars to go around.

As a result of this and other factors, the OSATs are consolidating. “(Consolidation) will bring a benefit to customers,” said Tien Wu, chief operating officer at ASE, in a recent interview. “If the industry players can consolidate, it will bring more R&D dollars (for packaging).”

Case in point: ASE recently announced plans to merge with Silicone Precision Industries (SPIL), the world’s third largest OSAT. Under the plan, ASE and SPIL will form a holding company. ASE and SPIL will be subsidiaries of the holding company. Through this arrangement, the two companies hope to pool their resources. That deal is still pending.

Then, earlier this year, ASE invested $60 million in Deca, a subsidiary of Cypress Semiconductor. ASE also will install Deca’s fan-out technology within its production plant in Taiwan. In addition to Deca’s technology, ASE is also working on five or so other fan-out package types. SPIL is working on at least three.

At the same time, the competition is working on a multitude of other fan-out packages, but the question whether there is room for everyone.

“This is going to be a ubiquitous technology and will consume a major portion of the existing flip-chip packaging market,” Deca’s Pycroft said. “The market will splinter and some companies will focus their fan-out solution on a given sector. The potential is there for over a dozen companies to be engaged.”