Scaling Options in Relation to 450mm

October 8, 2014

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Agenda

- Introduction
- Lithography
- 450 mm
- 3Di/Packaging
- Other semiconductors
- Smart phones surpass PCs in chip sales

- Leading-edge industry consolidation
  - Foundries; IDMs
  - Equipment suppliers

- How far/fast will scaling continue?
  - Continued scaling is cost driven
    (A. Manocha; Semicon West 2013)

Based On SRAM Size & Other Information Seen In Our Consulting Work. In Our View The “14nm” Nodes From Each Manufacturer Should Be Called:
- Intel – 16nm or 17nm
- Samsung – 18nm
- TSMC & GF – 20nm
- STM – 21nm

(Future Horizons, Semicon Europa 2013)
How can Moore’s Law be extended?

- **Performance / Power Consumption**
  - New materials
  - New devices
  - New architectures

- **Cost**
  - Lithographic scaling
  - Wafer size scaling
  - Chip stacking “3D”
How can Moore’s Law be extended?

- **Performance / Power Consumption**
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- **Cost**
  - Lithographic scaling
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[Image of graph showing litho costs back to normal with EUV >100 W/hr]

Mark Bohr, Intel.

[Images of Intel chip and ASML photo]

[Links and references provided]
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CNSE Albany Silicon Capabilities

- Full complement of 300 mm wafer tools
  - Leading-edge lithography
  - Backwards compatible to 65 nm; license
- Used today for 10-7 nm CMOS development
  - CNSE is a joint development partner
- Capacity of ~30 integrated wafer starts per day
  - 24/7 operation
- 1st 450mm tool set in the industry
Lithography Industry Challenges

- 193nm Cannot Meet Requirements for Scaled “7nm”

- 10nm Uses Patterning Tricks to Extend 193 Capability
  - Smaller CD but increasingly complex
    - Multiple-Pass Litho / Litho-Etch-Litho-Etch
    - Self-Aligned Double Patterning (Sidewall Image Transfer)
    - Source Mask Optimization Restrictions

- EUV Is Simpler and Potentially Cheaper @ 7nm Node
  - Min Feature Size ~15nm
  - Simplified Patterning
    - Single-Pass Litho Reduces Mask Count
    - Single SIT Processes
    - Wider Process Window
    - Bi-Directional Printing Possible
EUV Lithography Program

**EUV is gated by scanner productivity**
- A throughput of above 100 wafers/hr. is considered sufficient

**Other key infrastructure items**
- Actinic defect inspection (SEMATECH EMI program)
- Mask blank development (SEMATECH mask blank center)
- Resist Enablement Center access to MET and EUV full field
- Mask pellicle need / development

ASML 3300 at CNSE

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Development and Technology Intercept Targets

**G450C Program**

**Early 450 Development**

**ISMII: Early Si, Infrastructure**

**Tools for Consortium Demonstrations (unit process)**

**Start of std. Litho Capability**

**Test Wafers to support development and demo**

**G450C - Demonstrations:**
- 14nm
- 10nm
- 7nm

|------|------|------|------|------|------|------|------|------|------|------|------|
| 450mm implementation will require >10% cost benefit vs. 300mm
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- Full 2.5D/3D integrated process developed and implemented
- 3D DtW and WtW bonding
- Mid-via integration in 65 nm CMOS
- Fully customer tape-out ready

- Currently used, e.g., for integrated photonics on interposer
3Di Manufacturing Utica NY – SUNY IT

- **NYS Funded Packaging Facility**
  - RFE 10/15/2014

- **Technology Center for Standard and Advanced Packaging Manufacturing**
  - Provide packaging R&D consortia option for companies to interact and develop business opportunities
  - Offer quick turn facility for customer packaging applications
Key Challenges – Cost and Control

- **Top three process and equipment-related issues in 3D:**
  1. **Cost**
  2. **Cost**
  3. **Cost**
  4. No standards

- **Die-Wafer**
  - Speed of die attach process / tooling
  - Die level tracking
  - Process control

- **Wafer-Wafer**
  - KGD – test and overall yield
  - Die size matching

- **Alternatives?**
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Initial fab capacity 10k wafers/yr
Total fab output up to 1TVA/yr
The cost component of Moore’s law is running into head winds

The most significant options to continue manufacturing scaling:
1. EUV still has cost and infrastructure challenges to overcome
2. The transition to 450mm is projected toward the end of the decade
3. Chip stacking lacks standards and manufacturing cost issues remain

Many applications require less aggressive scaling
- Alternate substrates
THANK YOU