New Edge Exclusion Proposal

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Global 450mm Consortium, NY
Contents

- Background
- Wafer Status
- Metrology Status
- Process Status
- Summary
Edge Exclusion?

- **SEMI M55**
  - the width $X$ of a narrow band of wafer surface, located just inside the wafer edge, over which the values of the specified parameter do not apply

- **SEMI M59**
  - the distance from the FQA boundary to periphery of a wafer of nominal dimensions

- **Equipment or Material Supplier**
  - the edge area of a wafer that we cannot guarantee performance of our products

- **Chip Manufacturer**
  - the edge area that has been abandoned or forbidden from normal process
Edge Portion

- EE (Edge Exclusion)
- Fixed Quality Area
- Radius of FQA

✓ As Wafer Diameter Increases, Edge Portion Decreases
Edge Area

- 1mm EE Reduction Means
  - 0.9% Area Increase of 450mm
  - 1% Yield Increase Effect

- No EE of 450mm Means
  - 2.7% Area Increase of 450mm
  - 6.2% Increase Effect of 300mm

✓ No 450mm Edge Exclusion Equals 6.2% Area Increase of 300mm
# ITRS Roadmap History


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Manufacturer solutions are known


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Manufacturer solutions are NOT known

## Roadmap on Edge Exclusion Looks Going Backward
Current SEMI M1 Spec

- Basic Specification for 300mm Wafers
  - Was Nominal Edge Exclusion: \(3\text{mm}\), in 2011
  - Modified to Guide for Specification as \(148\text{mm}\) of FQA radius

- Specified Requirements for 450mm Wafers
  - FQA radius: \(223\text{mm}\)
  - Nominal Edge Exclusion: \(2\text{mm}\)

✓ Edge Exclusion Decreased To 2mm, Still Open to Dispute

\[\text{SEMI Standard M1-0413, Table R1-1}\]
Rome Wasn’t Built In A Day

- **1.5mm Edge Exclusion**
  - Earns Additional 700mm²
  - 0.45% of Total 450mm Wafer
  - 1.03% of Total 300mm Wafer

- **Beyond 1.5mm?**
  - Periphery
  - Edge width 0.35mm
  - EE 1.5mm
  - 1.15mm
  - FQA
  - ~ 1mm ??

- Barrier on 1mm: EBR, CMP, Litho, …

- **1.5mm Of First Step Dreaming Zero Edge Exclusion**
Reduced Exclusion Might…

✓ Increase Wafer Yield by 1.6%

300mm Pentium 4 Processor wafer
(130nm)

※ Kevin Fisher, Wafer Edge Exclusion
1.5mm EE Impact On # Of Chips

- **Shot Layout Simulation**

  - Shot Size: 26 x 8 mm
  - EE: 1.5mm or 2.0mm

<table>
<thead>
<tr>
<th>item</th>
<th>2mm EE</th>
<th>1.5mm EE</th>
<th>Delta</th>
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<tbody>
<tr>
<td># of full shots</td>
<td>684</td>
<td>688</td>
<td>+ 4</td>
</tr>
<tr>
<td># of partial shots</td>
<td>68</td>
<td>72</td>
<td>+ 4</td>
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<tr>
<td>sum</td>
<td>752</td>
<td>760</td>
<td>+ 8</td>
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</table>

- 4 Partial Shots May Be Newly Generated,
- 4 Partial Shots May Be Upgraded to Full Shots

- Changing EE From 2mm To 1.5mm May Increase 1% of # of Chips
Challenging Bottlenecks

- **Silicon Wafer Material**
  - *Silicon wafer edge flatness, roll off, roughness and etc.*

- **Metrology Capability & Reliability**
  - *Noise from edge boundary and optics limitation, beam size*

- **CMP Edge Removal Uniformity**
  - *Edge removal uniformity and removal rate decline comes from head limitation*

- **Photo Resist Edge Bead & Removal**
  - *Resist thickness uniformity controlling increased velocity and EBR clearance*
450mm Wafer Flatness

**SFQR**

- **SFQR Values**
  - Wafer Dependent
  - Usually Increase When EE Is Changed
    - From 2mm To 1.5mm
    - Wafer B Changed 22nm to 32nm
  - May Not Change
    - Wafer A Shows Similar SFQR

✓ 1.5mm EE May Not Make SFQR Worse
Edge Roll Off : ESFQR

- Significant ERO Changes Near Edge Region.
- SEMI M49 Nominal ESFQR Spec @ 1mm EE : 64 nm

※ Litho. Scanners require SFQR & ESFQR of the same magnitude in the printable radius (SEMICON Japan 2011).

✓ Edge Roll Off Is Challenging
Edge Roll Off: ZDD

- Defocus At Wafer Edge
- 450mm Wafer ZDD

- Defocus Variation Increases At EE > 3mm
- Wafer of Small ZDD Shows Best Distribution
- ZDD Depends on Wafers

- 450mm Wafer ZDD Shows Feasibility for Litho

† Takao Tamura et al, “Focus, Dynamics and Defectivity Performance At Wafer Edge in Immersion Lithography”, 2008
Edge Roughness Using AFM

- 450mm Bare Si Wafer Measured
- Scanned Area: 36um (6um x 6um)
- Roughness Increases At Edge

- No Significant Different Roughness Between 1.5mm & 2mm
Edge Metrology: Particle

- Particle Metrology Repeatability
  - Bare Si > 38nm, 20times
  - EE 1.0mm 95.55%
  - EE 1.5mm 95.55%
  - EE 2.0mm 95.52%
  - Total # of Particle Increases

- Current 450mm Particle Metrology Works At 1.5mm Edge

Specification: Repeatability shall be 98% or higher.

\[
\text{Repeatability(%) = \left(1 - \frac{\sigma}{\bar{X}}\right) \times 100}
\]

\[
\sigma = \sqrt{\frac{1}{n} \sum_{i=1}^{n} (X_i - \bar{X})^2}
\]

Xi: Defect count  \quad \bar{X}: Average of defect counts  \quad \sigma: Standard deviation
Edge Metrology: Ellipsometer

- **MSE & GOF of Thickness, LPCVD Poly Si**
  - MSE (Mean Squared Error) & GOF Values Are Stable At 1.5mm Edge
  - No Different N- or K- Value At Edge

- **N-Value & K-Value**
  - No Significant Difference Between 1.5mm & 2mm EE
Ellipsometer Variation Test

- **Variation 1.5mm vs. 2mm**
  - The Variation Is **NOT** Statistically Different

- **Variation 1mm vs. 2mm**
  - The Variation **IS** Statistically Different

- **Statistical Equivalence Between 1.5mm and 2mm EE**
Edge Metrology : XRF

- **Gauge R&R Test Method**
  - Cu Film Thickness with XRF
  - 1point @ 1.5 & 2mm edge
  - 50 times/day x 3days

- **Gauge R&R Test Result**
  - F Test Shows P-Value of 0.85
  - Two Distributions Are NOT Statistically Different

- XRF Has Equivalent Capability At 1.5mm & 2mm EE
Process Performance : CVD

- **PECVD SiN Thickness**

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<tr>
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<th>2.0mm EE</th>
<th>1.5mm EE</th>
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<tr>
<td><strong>Mean</strong></td>
<td>682 Å</td>
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<td><strong>Min</strong></td>
<td>677 Å</td>
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<td><strong>Max</strong></td>
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<td>694 Å</td>
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<td><strong>Std D / %</strong></td>
<td>3.20 Å / 0.47%</td>
<td>4.82 Å / 0.71%</td>
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- Edge Deposition Rate Slightly Goes Up

✓ PE-CVD Shows Feasibility Of 1.5mm EE Process
Process Performance: Metal

- TiN Thickness Per EE

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<tr>
<th>Thickness [Å]</th>
<th>1.0mm EE</th>
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<th>2.0mm EE</th>
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<td>Standard Dev. %</td>
<td>4.26 %</td>
<td>4.10 %</td>
<td>4.01 %</td>
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- Edge Deposition Rate Slightly Goes Down

- Metal Deposition Shows 1.5mm EE Feasibility
450mm Edge Bead Proposal

Immersion Trilayer Resist Stack

- Resist must fall on SiARC for adhesion & top coat must encapsulate resist.
- Wafer edge expose (WEE) of 1.5mm can be applied prior to develop.

✓ Trial To Get 1.5mm Edge Bead Process Has Been Started
Time Line For 1.5mm EE

- **Modification Of SEMI Standard**
  - M1 FQA Radius From 223mm To 223.5mm
  - Collaborating With SEMI Si Committee, PW TF, AWG TF and 450mm Wafer TF
  - Combining With Silicon Wafer Notch-less Activities
  - Focusing on 450mm, Possibility Of Extension Into 300mm

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- **Basic Evaluation**
  - Metrology & Material

- **Advanced Assessment**
  - Bottle Neck Process Feasibility

- **Official Proposal**
  - SEMI Standard Meeting
  - SEMICON West

- **Submit SNARF**
  - SEMI Standard Meeting
  - SEMI 7th Cycle

- **Ballot Adjudication**
  - SEMI Si Committee
  - SEMICON Japan
Summary

- **Purpose**
  - To Maximize Cost Effect of 450mm Transition By Getting More Area

- **Material**
  - Current Wafer Edge Roll Off Status Shows Feasibility of 1.5mm EE

- **Metrology**
  - Basic 450mm Metrology Can Support To Develop 1.5 EE Equipment & Process

- **Process Equipment**
  - Some Process Show Feasibility, Some Need Improvement

- **Plan**
  - Modification of SEMI Standard M1 EE By The End Of 2013
**Special Thanks To**

- **G450C Metrology Team**
  - Dr. Rand Cottle, Mr. Jeffrey Lee, Ms. Katherine Sieg, Mr. Nithin Yathapu

- **SEMI**
  - Mr. James Amano

- **SEMI Standard International Advanced Wafer Geometry TF**
  - Dr. Jaydeep Sinha

- **SEMI Standard International 450mm Wafer TF**
  - Dr. Michael Goldstein

- **SEMI Standard International Polished Wafer TF**
  - Dr. Murray Bullis / Dr. Noel Poduje
Thank you.