Stronger partnerships: Reducing risks, accelerating progress

Jim Koonmen, SVP ASML
Silicon Valley Lunch Forum, 25 April 2013
Agenda

• Partnerships 2.0 – Accelerate and de-risk new technologies
• EUV – Progress and update
• Immersion – Double patterning update
• 450 mm update
• Summary and conclusions
It’s all about trust

Trust = \frac{\text{Capability} \times \text{Transparency} \times \text{Reliability}}{\text{Self-Interest}}
Deeper partnerships throughout the value chain

Suppliers should understand customer needs
Customers should understand supplier capabilities
Partnerships drive the right balance
Customer Co-Investment Program: Rationale

- Industrialization of EUV Lithography and transition to 450 mm are essential enablers for Moore’s Law and deliver the required economic benefits.
- Increasing complexity and huge investments make it necessary to have risk sharing amongst customers and suppliers.

Sharing the risk:
Technology funding €1.38B

Sharing the reward:
Equity participation €3.85B
Acquisition of Cymer

Merging ASML and Cymer:

• Creates efficiency in EUV technology development
• Accelerates Industrialization of EUV source
• Simplifies EUV source supply chain
• Optimizes manufacturing flow of EUV modules
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Industry roadmap towards < 10 nm resolution
Lithography supports shrink roadmap

* Note: Process development 1.5 ~ 2 years in advance
updated Dec/12
<table>
<thead>
<tr>
<th></th>
<th>NXE:3100</th>
<th>NXE:3300B</th>
</tr>
</thead>
<tbody>
<tr>
<td>NA</td>
<td>0.25</td>
<td>0.33</td>
</tr>
<tr>
<td>Illumination</td>
<td>Conventional 0.8 σ</td>
<td>Conventional 0.9 σ Off-axis illumination</td>
</tr>
<tr>
<td>Resolution</td>
<td>27 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>Dedicated Chuck Overlay / Matched Machine Overlay</td>
<td>4.0 nm / 7.0 nm</td>
<td>3.0 nm / 5.0 nm</td>
</tr>
<tr>
<td>Productivity</td>
<td>6 - 60 Wafers / hour</td>
<td>50 - 125 Wafers / hour</td>
</tr>
<tr>
<td>Resist Dose</td>
<td>10 mJ / cm²</td>
<td>15 mJ / cm²</td>
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The **NXE:3100** has exposed >30,000 wafers

Enabling customers to go through cycles of learning
Eleven NXE:3300B systems in various states of integration

*New clean room completely finalized in July 2012*

System 1: 
System 2: 
System 3: 
System 4: 
Development tool 
System 5: 
System 6: 
System 7: 
System 8: 
System 9: 
System 10: 
Training
NXE:3300B imaging and overlay beyond expectations

**Scanner qualification**

- BE = 15.9 mJ/cm²
- EL = 13%
- DoF = 160 nm

- Full wafer CDU = 1.5nm

**Scanner capability**

- 22nm HP
- 13 nm HP
- 18 nm HP
- 23 nm HP

- NXE- immersion [nm]

**Matched Machine Overlay**

- Lot (1.3,1.3)
- Lot (3.4,3.0)

**Dedicated Chuck Overlay [nm]**

- Day
- Wafer

- 1 nm
- 2 nm
- 3 nm
- 4 nm
- 5 nm
- 6 nm
- 7 nm
- 8 nm

- 22nm HP
- 13 nm HP
- 18 nm HP
- 23 nm HP

- Scanner qualification
- XT:1900i reference wafers
- EEXY sub-recipes
- 18par (avg. field) + CPE (6 par per field)

- Full wafer CDU = 1.5nm

- Scanner capability
NXE:3300B - Good imaging performance logic metal1

~10 nm logic node, minimum half-pitch 23 nm, single exposure printing
EUV Source Power Progress reaching 55 W
Supporting 43 wafers/hour, 250 W target to be reached in 2015

- At 55 W, 1 run: 97.5% of the dies < 0.5% dose
- At 40 W, 6 runs: 99.99 of the dies < 0.2% dose,
- 7 one hour runs total representing ~ 250 exposed wafers @ 15 mJ/cm²
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ArF immersion for cost-efficient Double and Quadruple Patterning
NXT platform will be ready for all critical layers

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</thead>
<tbody>
<tr>
<td>On Product Overlay</td>
<td>9 nm</td>
<td>6 nm</td>
<td>4 nm</td>
<td>3 nm</td>
</tr>
<tr>
<td>CD Uniformity iso</td>
<td>3 nm</td>
<td>1.5 nm</td>
<td>1 nm</td>
<td>&lt;1 nm</td>
</tr>
<tr>
<td>Total Focus Budget</td>
<td>100 nm</td>
<td>80 nm</td>
<td>60 nm</td>
<td>&lt;60 nm</td>
</tr>
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<tbody>
<tr>
<td>DCO / MMO</td>
<td>2.5 / 5.5 nm</td>
<td>2.5 / 4.5* nm</td>
<td>2.0* / 3.5* nm</td>
<td>&lt;1.5* / &lt;2.5* nm</td>
</tr>
<tr>
<td>Full Wafer Focus Unif</td>
<td>30 nm</td>
<td>22 nm</td>
<td>20 nm</td>
<td>15 nm</td>
</tr>
<tr>
<td>Full Wafer CDU (iso)</td>
<td>3.0 nm</td>
<td>2.0 nm</td>
<td>1.3 nm</td>
<td>1.0 nm</td>
</tr>
<tr>
<td>Throughput (96 shots)</td>
<td>190 WpH</td>
<td>230 WpH</td>
<td>250 WpH</td>
<td>250 WpH</td>
</tr>
<tr>
<td>Defects/Wafer</td>
<td>10</td>
<td>10</td>
<td>&lt;7</td>
<td>&lt;7</td>
</tr>
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</table>

* Full Wafer to reference
Holistic lithography supports shrink roadmap

Process window enlargement
- OPC / OPC verification
- Illumination / wave front / mask optimization
- Application-specific corrections

Process window control
- Baseline + stand alone metrology to maintain scanner stability and matching
- Optimizers + integrated metrology to correct layout and process influences
Integrated Metrology is the only viable way to control volume production for 20 nm process and below
Integrated Metrology drives on product performance improvements

4 Key technical differentiators:
- Integration on Track
- Measurement accuracy with diffraction-based overlay
- Small targets for in die measurements
- Focus measurement with asymmetric targets

0.9 nm OPO improvement measured
30% focus uniformity improvement
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The promise of larger wafers

<table>
<thead>
<tr>
<th>Size</th>
<th>Wafer Area</th>
<th>Effective Area</th>
<th>Cost Reduction Goal</th>
</tr>
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<tbody>
<tr>
<td>200 mm</td>
<td>2.25X</td>
<td>2.36X</td>
<td>30%</td>
</tr>
<tr>
<td>300 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>450 mm</td>
<td>2.25X</td>
<td>2.40X</td>
<td>30%</td>
</tr>
</tbody>
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Source: Shang-yi Chiang, TSMC, SPIE March 2011
Lithography is at the heart of chip manufacturing.

450 mm wafers only provide limited cost benefit for scanning systems.

Non-scanning process equipment can provide cost advantage from wafer size increase to 450 mm.

Scanning (lithography) systems provide limited cost benefit from wafer size increase to 450 mm.
Silicon area patterned per hour is comparable for 300 mm and 450 mm lithography tools.

450 mm wafer throughput is ~50% of 300 mm wafer throughput.
Litho economics 300 mm => 450 mm challenging

New technology needed to stay neutral in cost

<table>
<thead>
<tr>
<th>Throughput</th>
<th>Relative cost</th>
</tr>
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<tbody>
<tr>
<td>WpH m2/H 450/300 mm</td>
<td>Cost/ m2</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>300 mm limit</td>
<td>250 18</td>
</tr>
<tr>
<td>450 mm linear stage scaling</td>
<td>100 16</td>
</tr>
<tr>
<td>450 mm new technology</td>
<td>125 20</td>
</tr>
</tbody>
</table>

New 450 mm technology to balance cost (productivity) & performance (overlay)

Throughput ↓

300 mm limit: 250 WpH, 18 m2/H, 1.0 cost, 1.0 cost/m2, 100%

450 mm linear stage scaling: 100 WpH, 16 m2/H, 0.9 cost, 1.1 cost/m2, 122%

450 mm new technology: 125 WpH, 20 m2/H, 1.1 cost, 1.1 cost/m2, 100%
450 mm for productivity and cost

- Customers increasingly concerned about manufacturing cost. ASML will enable continuous cost reduction, primarily through shrink. Shrink becomes a bigger risk for our customers given the overall technology risk. 450 mm looks like a doable cost reduction scenario.

- 450 mm wafers provide limited cost benefit for scanning systems

- Significant enhancements in overlay are required next to wafer size increase to accommodate the roadmap

- ASML has engaged with a funding program over the next 5 years with its major customers to accelerate their development programs including 450 mm

- ASML has initiated 450 mm program on 2 platforms and 4 wavelengths

- Early version tools in 2015/16, volume systems in 2018

- Overall concern remains due to limited overall industry 450 mm implementation plans
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Affordable shrink roadmap

Performance scaling on Immersion litho:
- On Product Overlay (OPO) <8.5 nm → < 3 nm
- Critical Dimension Uniformity (CDU) <2.0 nm → 1 nm
- Throughput 200 wafers per hour (wph) → >250 wph

Economics and extendibility of EUV:
- Resolution 22 nm → 8 nm
- EUV to immersion overlay 5.0 nm → 2 nm
- Throughput 70 wph → >125 wph

Cost opportunity of 450 mm:
- Boost die throughput
- No litho cost increase per die
Summary and Conclusions

• In combination with a holistic approach, immersion technology is capable of supporting shrink to 14 & 10 nm:
  • Optimization of mask, illuminator (FlexRay) and pupil (FlexWave)
  • Integrated Metrology with Yieldstar

• Once power is sufficient for 125 wafers per hour, EUV becomes technology of choice for high volume production of key layers
  • Key resources and stake holders aligned through co-investment program and Cymer acquisition

• Industry aligning on 450 mm insertion point around 10 nm node
  • “EUV first, 450 mm later”

• More / deeper partnerships required throughout the industry to maintain speed and affordability