Agenda

In this presentation I will show:

- K&S company overview
  - What solutions we offer for the Semiconductor Assembly Equipment market
  - European Innovations and competitive manufacturing
  - Technological Highlight
    - What makes us different, What are we especially good in
    - How does this help to stay in Europe

- K&S Hybrid machine
  - Single machine solution for combined Flip Chip and SMD assembly

- Q&A
About Kulicke & Soffa (K&S)

Global Technology & Market Leader in Semiconductor Assembly Equipment

- Founded in the US in 1951 and incorporated in 1956
- Publicly traded since 1971 in NASDAQ: KLIC
- Strong presence in Asia with over 80% sales in Asia
- HQ in Singapore since 2010
- Acquisition of Assembleon January 9, 2015, Assembleon becomes a business line of K&S
- Over 2500 employees
# Semiconductor Assembly Equipment

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<th>Semiconductor</th>
<th>Hybrid</th>
<th>Beyond Semi</th>
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<td>Advanced Packaging</td>
<td>Advanced SMT</td>
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<td>Wedge Bonding</td>
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<td>Embedded Die</td>
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<td>SIP</td>
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- **Advanced Packaging:**
  - Flip Chip
  - WLP
  - FOWLP
  - PoP
  - Embedded Die
  - SIP

- **Technology Innovation Solutions**
Global Presence

Switzerland, Berg
Advanced Packaging and
Software R&D

Veldhoven, Netherlands
Advanced Packaging,
Advanced SMT, R&D and
Manufacturing

Brazil, Brazil
Advanced Packaging
R&D

USA, Fort Washington (PA)
Equipment R&D
Advanced Packaging R&D

USA, Santa Ana (CA)
Wedge Bonder R&D

China, Suzhou
Bonding Tools Manufacturing
Blades R&D, Manufacturing
Software R&D, Advanced
Packaging, Advanced SMT

Singapore (Corporate HQ)
Ball Bonder, Wedge Bonder,
Wafer-Level Bonder,
Advanced Packaging, Advanced SMT,
R&D and Manufacturing

K&S Manufacturing Plant
K&S R&D Center
K&S Sales/Service Office
Two Advanced Packaging BLs

**AP (Local Reflow) BL**

Thermo-compression

K&S APAMA

**AP (Mass Reflow) BL**

WLP/FOWLP
Flip Chip
Embedded Die
Module
Package-on-Package
System-in-Package

K&S HYBRiD

Reflow

Bonded Die

Bonded Die Or Chip
K&S Hybrid Machine

- Most advanced tool for applications combining FC’s & SMD’s
- Ideal solution for:
  - SIP, Modules, MEMS, WLP, FOWLP, POP, etc.
- Best cost per unit ratio (total unit, FC & passives combined)
- Different transport systems for regular PCB’s, wafers or panels up to 800 x 457, Vacuum Transport, Carrier transport, lead frames
- Largest component range from 0.2x0.2mm – 45x45mm
- Scalability within one machine
  - UPH: up to max 15K for FC or > 120 K for SMD’s or any combination
  - Accuracy: Between 25µm & 7µm creating optimum combination of accuracy & UPH
How does this help to stay in Europe

Competitive Manufacturing:

- Cost of manufacturing is mainly defined by:
  - Cost of equipment, which is about the same anywhere in the world
  - Operational cost
    - Majority of the cost is related to labor and energy
  - Efficiency of manufacturing (output vs cost)

- To improve the cost per unit:
  - Minimize the cost
    - Minimize the energy consumption
    - Minimize the need for operators
  - Maximize the throughput of a production line
    - Maximize manufacturing line efficiency
Minimize the energy consumption

“The greenest pick and place solution”

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<tr>
<th>Machine type</th>
<th>K&amp;S Hybrid</th>
<th>Comp. A</th>
<th>Comp. B</th>
<th>Comp. C</th>
<th>Comp. D</th>
<th>Comp. E</th>
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*: Based on 100K CPH in a year
Maximize manufacturing line efficiency

**SIP Assembly Process Flow (Flip Chip) – traditional**  (15 steps)

**SMT department**
- Stencil Paste
  - Place SMD
  - reflow
  - Tray Load

**BE department**
- Tray UnLoad
  - Flip Chip attach
  - Clean
    - reflow
    - Cure
  - Laser Mark
    - Cure
    - Mold
    - Plasma Clean
  - Singulation
    - Tray Load for Test
    - Tray Load
Maximize manufacturing line efficiency
SIP Assembly Process Flow (Flip Chip) – NEW (12 steps)

Stencil Paste → Place SMD → Flip Chip attach → Reflow → Clean

Laser Mark → Cure → Mold → Plasma Clean → Cure

Singulation → Tray Load for Test

Both activities in one department
Maximize manufacturing line efficiency
Wafer Level Packaging

Combining Flip Chips and Passives onto 300 mm wafers

- Placement of Flip Chip’s fed from wafer feeding and passives like 0201, 01005 or 008004 (0201metric) fed from tape feeders and onto a 12” wafer frame

- Example Project:
  - > 900 circuits/wafer, each with 1 FC & 28 passives: Total > 26 K placements / wafer
Decreasing the cost of manufacturing

Traditional manufacturing
2 individual process steps

- FC’s bonded by Semicon machines
  - High accuracy (< 10 μ)
  - UPH: max 5 K UPH
  - Feeding from wafer
  - Capable of bonding thin dies
  - High cost per unit

- Passives placed by SMD machines
  - Accuracy around 25 – 50 μ
  - UPH: > 100 K UPH possible
  - Feeding from tape and reel
  - Low cost per placement

K&S Hybrid machine
Single machine solution

- One modular system combining FC bonding and passive placement
  - Accuracy up to 7 μ for FC placement
  - UPH up to 15 K for FC’s or 120 K for passives or any combination
  - Feeding from wafer, waffle pack, JEDEC tray, tape and reel, etc
  - Full controlled placement force for low profile passives

K&S Hybrid, best of both worlds:
- High end, fast FC bonding
- Low cost passive placement
Decreasing the cost of manufacturing

K&S Hybrid, single machine solution for SMT + Flip Chip assembly:

- Less material handling
- Less operators
- Less (cleanroom) floor space
- Less training
- Less maintenance
- Less Vendors
- Less process steps
- Lower capital investment
- Lower running cost
- Higher Efficiency
- Higher intrinsic quality
- Single pass reflow / curing

K&S Hybrid, best of both worlds:
- High end, fast FC bonding
- Low cost passive placement
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