Moore’s Law and beyond, 3D-IC Design Infrastructure Enablement

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Outline

• Semiconductor challenges – More Moore or beyond Moore?
• Emerging 3D-IC technologies
• 3D-IC methodology
• Conclusions
More Moore? Or More Than Moore?
It’s a Bimodal World
Chip design – a bimodal world

Source: UBM TechInsights (EETimes, October 2012)
Chip design – a bimodal world

Many design starts
Low NRE
Many sockets
Lower ROI
High volume
Low premium

Few design starts
High NRE
Few sockets
High ROI
High volume
High premium

Source: IBS 2012
# Cost of advanced-node designs

<table>
<thead>
<tr>
<th>Source: IBS, May 2011</th>
<th>32 / 28nm node</th>
<th>22 / 20nm node</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fab construction</td>
<td>$3B</td>
<td>$4B – 7B</td>
</tr>
<tr>
<td>Process R&amp;D</td>
<td>$1.2B</td>
<td>$2.1B – 3B</td>
</tr>
<tr>
<td>Design cost</td>
<td>$50M – 90M</td>
<td>$120M – 500M</td>
</tr>
<tr>
<td>Mask set</td>
<td>$2M – 3M</td>
<td>$5M – 8M</td>
</tr>
<tr>
<td>EDA enablement</td>
<td>$400M – 500M</td>
<td>$800M – 1.2B</td>
</tr>
</tbody>
</table>

Design cost: ~$200M
Need product opportunity > $1B
One way to get around this:
Disruptive analog design (More Moore)

- Difficult to do analog design at advanced nodes
  - Layout restrictions
  - Transistors good for digital, not great for analog
  - Variation
- New approaches
  - Digitally-assisted analog
  - Digital implementation of analog functions

Example: fully digital analog RF power amplifier at 40nm

Source: Ali Niknejad, 2012
3D-IC is a bridge for "More Than Moore" solutions

Source: UBM TechInsights
(EETimes, October 2012, May 2011)
Why 3D?

- **Package Size:** 35%
- **Power Consumption:** 50%
- **Bandwidth:** 8x

**POP**
- Conventional PoP Solution (Package-on-Package)

**3D TSV**
- Direct chip connection using TSV (TSV-micro bump joint)

Source: Samsung Electronics 2012
Emerging 3D-IC Technologies: Proof Points
Short-, medium-, and long-term path to 3D-IC

EDA work starts at least 3-4 years earlier

**Si Partitioning with TSV Interposer**
- Market: FPGA
- Xilinx in 2010
- 2011-2012

**Memory Cube with TSVs**
- MARKET: Server and computing
- IBM and Micron
- 2012-2013

**Logic + memory w/ 2.5D TSV Interposer**
- MARKET: GPU, gaming console
- ST testchip in 2010
- 2013-2014

**Wide IO + Logic with TSVs**
- MARKET: Mobile, tablet, gaming processors
- ST-E / LETI WIOMING in 2011
- 2013-2014

**High-performance computing**
- MARKET: CPU, MCMs etc
- ST-E / LETI WIOMING in 2011
- ~ 2015

**Standards, ecosystem, cost**
Homogenous stack of dies on interposer

- **Why?**
  - Yield gains
- **Design enablement**
  - Stretch existing tools
  - Bump creation / alignment
  - Electrical analysis

*Example: Xilinx Virtex 7-2000T*

Source: L. Madden, Xilinx, 2011
Hybrid memory cube

• Why?
  – Increased bandwidth
  – Power efficiency
  – Smaller size
  – Scalability and reduced latency

• Design enablement
  – Stretch existing tools
  – Electrical analysis
Memory and logic on interposer

- Heterogeneous stack of dies on interposer
- Design enablement
  - Die assembly tools, bump / TSV placement
  - Electrical analysis
  - Thermal analysis
Why?
- Bandwidth
- Design enablement
  - Die assembly tools, bump placement
  - Electrical analysis
  - Thermal analysis

Wide IO memory on logic stacks
Memory “Cube” on logic

• Why?
  – Next generation of memory / logic integration

• Design enablement
  – Need to investigate additional requirements
3D-IC Methodology: What does it take?
3D-IC design flow challenges

New 3D-IC design flow challenges

- System-level exploration
- 3D floorplan – optimized power plan and TSV / bump locations
- Implementation placement, optimization and routing
- Extraction and analysis
  Manage power, thermal and SI
- DFT for 3D-IC stack and diagnostics
- Silicon package co-design
3DIC Owner-Aligned Solutions

SOC/Digital entry point

- EDI
- Sigrity
- Allegro
- PVS
- QRC
- ET
- RC
- Virtuoso

System entry point

- Allegro
- EDI, Virtuoso
- Sigrity
- Spectre
- UltraSim
- PVS
- Wide IO
- QRC
- RC
- ETS
- ET
- EPS

Virtuoso entry point

- Virtuoso
- Sigrity
- PVS
- Spectre
- ETS
- Wide IO
- ET
- RC
- UltraSim
- EPS
- Allegro
- QRC
3D-IC design flow challenges: System-level exploration

- **What is the optimal architecture?**
  - Design partitions
  - Technology node for each die
  - Die orientation, bump / TSV styles
  - Block selection:
    - Which block goes into which die (DDR, display control, transmitter, DC converter, DAC, etc.)

- **What if analysis**
  - Performance (delay, latency)
  - Power, thermal
  - Mechanical stress

- **Cost: turn-around time**

Optimize system cost with shortest TAT
3D-IC design flow challenges:
3D-Aware die floorplan

- Co-design between package and IC stack for optimized TSV and bump locations
- Cross die bump optimization
- Optimizing power plans

<table>
<thead>
<tr>
<th>Device</th>
<th>Data source</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA</td>
<td>BGA.txt from Cadence APD</td>
</tr>
<tr>
<td>Si interposer</td>
<td>Created on-the-fly</td>
</tr>
<tr>
<td>Die slice 1</td>
<td>LEF / OrbitIO IOview</td>
</tr>
<tr>
<td>Die slice 2</td>
<td>ASCII data</td>
</tr>
</tbody>
</table>

Multi-fabric planning view

Bump pattern development and RDL routing and editing

Export interfaces to IC detailed implementation tools
3D-IC implementation: An interposer example

- Mother die:
  - Digital;
  - Bump location exported from digital implementation tool

- Daughter die:
  - Full custom;
  - Bump location exported from custom implementation tool

- Interposer:
  - Full custom;
  - Implemented in custom design tool
Configuring the stack

Top view

Cross section
Visualization of mother / daughter die
Checking bump alignment
Routing interposer
Die / interposer co-design

Editing daughter_die
Background: interposer

Editing interposer
Background: daughter_die
3D DFT requirements

• Pre-bond test
  – Focus on die-internal circuitry
  – Original thick or thinned-down wafer
  – Probe access at DUT
  – Probe on micro-bumps or dedicated pads

• Mid-bond / post-bond / final tests
  – Focus on interconnects and die-internal circuitry
  – Test access (probe or socket) at bottom die
  – Require DFT to propagate test stimuli / responses up / down through stack
  – Requirements
    – Modular test: core, die, interconnect
    – TestTurn: test up till this die
    – TestElevator: test higher-up die
3D DFT architecture

Example functional design

- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins
3D DFT architecture

Example functional design
- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

Example existing design-for-test
- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Stack product: IEEE Std 1149.1
3D DFT architecture

Example functional design
- \( \geq 2 \) stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

Example existing design-for-test
- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Stack product: IEEE Std 1149.1

3D DFT architecture
Test wrapper per die
- Based on IEEE 1149.1 or 1500
- Two entry / exit points per die:
  1. Pre-bond: extra probe pads
  2. Post-bond: extra TSVs

[Marinissen et al. – VTS’10 / 3DIC’10]
3D-IC electrical analysis: example

Silicon Interposer Example

- Three chips are placed faced down on top of silicon interposer.
- Silicon interposer: 4-9 levels of high density Interconnect.
  - No active areas.
  - Passive devices like metal capacitances.
- Challenges: Physical design, electrical analysis, power distribution and analysis and thermal management.
IR drop analysis: flow

IR DROPP Analysis (flow)

- Power Mesh
  - Extracted RC(L)

- 3D-IC Design Data

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Voltage Drop Analysis
(Static, dynamic, etc.)

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Power Drop Reports

- Micro-bump and TSV are modeled as RC or RLC.
- Analysis of all chips are the same time to provide accurate analysis.
- Design data includes physical design data for 3D-IC
- Results are provide on all data, including 3D -IC components.
IR drop analysis: models
IR drop analysis: results

- The white points are the feedthrus which pass power to the die1 and die2. User can also zoom in to check the IR drop on feedthrus.
Thermal analysis: flow

- Analysis of all chips at the same time to provide accurate analysis.
- Using the 3D-IC layer Stack Technology File.
- Design data includes physical design data for 3D-IC.
- Results are provided on all data, including 3D-IC components.
Cadence 3D-IC Integrated Solution

Complete Implementation Platforms for flexible Entry Point and Seamless Co-design

Using OpenAccess, EDI, Virtuoso each has dedicated 3DIC functions that work together, plus co-design with Cadence SiP tools for complete End to End implementation including early stage system exploration and feasibility.

Full Spectrum Analysis Capability

- RC/ET DFT and ATPG for 3DIC
- EPS/ETS/QRC Digital Analysis Tool
- Virtuoso Based Full Spice Simulation Capacity
- SiP/Sigrity based Extraction, SI, and PI System/Package Analysis

Ecosystem partnership and Real Experiences/Proof Points

Cadence has been working with ecosystem partners since 2007 on 3DIC
- 8 test chips completed and 1 production chip done
- Several projects ongoing
Summary
3D integration challenges

- Economical 3D stacking in high-volume manufacturing presents many challenges
- Benefits must exceed the additional costs of TSVs, and yield fallout
- Logistics of testing and assembling die from multiple sources can be substantial
- Systematic and integrated EDA enablement are needed
Collaboration is key to success
3D-IC ecosystem and collaborations

Designers: analysis driven design and stacking methodology

EDA: design tools to implement methodology

System house: multi-die integrated package prototyping

Foundry / IDMs / OSAT / interposer / package: Rules, stacking Layers and modeling

Everyone: Cost models, DFM / yield / reliability and redundancy
A message to European academia

- Cadence is making its 3D-IC design tools available to selected European academic institutions in partnership with the Europractice scheme operated by the UK Science and Technology Facilities Council Rutherford Appleton Laboratory

- Proposals are being invited from the existing Europractice/Cadence user base of 378 European academic institutions

- These selected early adopters will then be able to more efficiently design 3D-IC systems for their research projects, e.g. in new computer architectures, with the possibility of fabrication via existing broker services offered by CMP ( Circuits Multi-Project) in France
Backup
Thermal analysis: results

Thermal Analysis Results

- Thermal Analysis Provides a Rich of Thermal Data
  - 2D Thermal contour can be displayed on each chip.
  - 3D Thermal Map.
  - Thermal values per layer and per x,y coordinates.
- The example below has small power consumption $\Rightarrow$ thermal gradient is small

![The temperature distribution contour map](image1)

![The 3D plot of the temperature](image2)
EDA for 3D-IC: current status

• Some designs can be done with existing tools
• More sophisticated implementation and analysis tools are being developed
  – Examples shown before
• Gaps exist
  – Path-finding
  – System analysis and optimization with implementation details
• No fundamental limitations: economics dictate rate-of-tool development
3D-IC design flow challenges: System-level electrical analysis

- Interposer electrical performance assessment
  - Near-field results for 500Mhz
  - Package / board model extraction
  - Chip and interposer model extraction
  - SSO system co-analysis results
  - Co-analysis for emissions
  - Frequency Domain Results through FFT
  - Far-field Radiation
  - Near-field Radiation
  - E-field observed 5mm above top of the package
    E-fields at 500Mhz and 1GHz are reduced by about 80%

- Circuit import from LEF/DEF
  - Memory Die
  - Logic Die

- Transient Co-Analyses of Chip-Interposer-Package System
  - 100mV noise with only 8-bits randomly switched.
  - Non-ideal PDM has significantly greater noise and more timing jitter.

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So what changes with 3D-IC in EDA world?
Revamped EDA requirements

- New layout rules (e.g. alignments)
- New layout layer (e.g. back-side RDL)
- New layout and electrical feature (e.g. TSV)
- New floorplanning and blockage rules (TSV)
- Thermal and mechanical constraints
- New models, rules

Courtesy: Qualcomm