DSA: Progress Toward Manufacturing Readiness

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Senior scientist, CEA-Leti, France
3 LITHO PROGRAMS IN LETI

ONE FOCUS
DEVELOP **LOW COST** PATTERNING SOLUTIONS
Graphoepitaxy for contact

Graphoepitaxy for L/S

Chemoepitaxy for L/S

First high chi evaluation

22nm < \(L_0\) < 60nm

L_0 < 20nm

Technological Flow:

**Materials:**
- ✓ PS-\(b\)-PMMA \(L_0 = [25:55]\)nm
- ✓ Neutral layer
- ✓ High chi BCP \(L_0 < 25\)nm

300 mm Process Line:
- Lithography for guiding patterns
  - 193 i or e-beam
- DSA dedicated track
  - Specific bake
  - Solvent annealing
  - PMMA removal step
- Dedicated metrology
  - CD-SEM
  - SP2

Integration:
- Compact and physical model
- Shortloops with ST
- Dedicated defectivity tools
Balancing BCP Thickness over Template Density in Graphoepitaxy

All images are taken on the same processed wafer

DSA Planarization: Full control of BCP self-assembly through pitch
Balancing BCP Thickness over Template Density in Graphoepitaxy

**Champion wafer**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD mean</td>
<td>17 nm</td>
</tr>
<tr>
<td>CDU wafer 3σ</td>
<td>1.3 nm</td>
</tr>
<tr>
<td>PE-3σ</td>
<td>1.3 nm</td>
</tr>
<tr>
<td>Nb of defects</td>
<td>0 defects/cm²</td>
</tr>
<tr>
<td>Inspected area</td>
<td>0.01 mm²</td>
</tr>
<tr>
<td>Nb of inspected contacts</td>
<td>$6 \times 10^5$</td>
</tr>
</tbody>
</table>

**DSA planarization**: A full control of the template density over the wafer
The POR used to implement statistical monitoring

**SEMICON EUROPA**
14-17 NOV 2017
MUNICH GERMANY

**Resist**
**SiARC**
**SOC**
**Metal**
**Oxide**
**Substrate (Si)**

**Guiding pattern**
(193i litho)

**BCP over-thickness filling**

**Self-assembly annealing**

**Etch-back & PMMA removal**

**Surface preparation**

**PS**
**PMMA**

**200nm**
300 mm Process Stability Monitoring

**FINGERPRINT**

- **BCP coating**
  - Thickness per run (nm)
  - Target (@48.3nm)
  - Target - 3sigma
  - Target + 3sigma

  ![BCP coating graph](image)

- **Natural period L₀**
  - L₀ per week
  - Target (@35nm)
  - Target - 3sigma
  - Target + 3sigma

  ![Natural period L₀ graph](image)

**PATTERNED SURFACE**

- **CD & CDU**

  - CDU wafer inter-chip
  - CD_mean

  ![CD & CDU graph](image)

- **HOY & placement error (PE)**

  - PE_3s
  - HOY(%)

  ![HOY & PE graph](image)

**POR on SOKUDO DUO Track using C35 from Arkema**

- Fingerprint: Thickness (NL and BCP); BCP’s L₀ and CD
- Grapho: CD, CDU, PE, HOY
Inorganic template: a reworkable process

- Rework of DSA litho step
- Thermal stability
- Better surface affinity control

**Inorganic templates added value**

### DSA
- Pitch 120 nm
- Stat (800 contacts)
- DSA:
  - CD = 18.0 nm
  - CDU-3σ = 1.4 nm
  - HOY = 100%

### DSA + rework + DSA
- Pitch 120 nm
- Stat (800 Contacts)
- DSA:
  - CD = 18.0 nm
  - CDU-3σ = 1.3 nm
  - HOY = 100%
# Inorganic vs Organic template

## SIARC/SOC
### Organic template

<table>
<thead>
<tr>
<th>SIARC</th>
<th>SOC</th>
<th>Guide template: CD guide = 40.5 nm</th>
<th>CDU-3σ guide = 4nm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>DSA:</strong> CD = 17.2nm</td>
<td>CDU-3σ = 1.3nm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Residue ~ 7nm</td>
<td>HOY = 100%</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Rework:</strong> NO</td>
<td><strong>Planar:</strong> OK</td>
</tr>
</tbody>
</table>

## Silicon Oxide
### Inorganic template

<table>
<thead>
<tr>
<th>Silicon Oxide</th>
<th>Guide template: CD guide = 40 nm</th>
<th>CDU-3σ guide = 4.6nm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>DSA:</strong> CD = 17.6 nm</td>
<td>CDU-3σ = 1.4nm</td>
</tr>
<tr>
<td></td>
<td>Residue ~ 7nm</td>
<td>HOY = 100%</td>
</tr>
<tr>
<td></td>
<td><strong>Rework:</strong> OK</td>
<td><strong>Planar:</strong> OK</td>
</tr>
</tbody>
</table>

Equivalent DSA performances were achieved with inorganic guiding template.
Embedded neutral layer: fingerprint

To accurately control the polymer residue: selective neutral layer (NL) on the template bottom side

1/ NL grafting
2/ Sacrificial layer deposition
3/ Sacrificial layer removal
4/ BCP spin coating
5/ BCP thermal assisted Self-assembly
The sacrificial layer is successfully integrated in the new integration flow.
Embedded neutral layer: DSA

**NL residue thickness:** 8 nm ($3\sigma = 0.6$ nm)

**NL thickness can be reduced by** $\downarrow M_w$ (e.g. 3 nm)

Uniformity & thickness control of the residue is achieved !!!
Comparative evaluation / PoR vs New integration

<table>
<thead>
<tr>
<th></th>
<th>PoR</th>
<th>Embedded NL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD mean</td>
<td>18nm</td>
<td>22nm</td>
</tr>
<tr>
<td>Guiding CD</td>
<td>40nm</td>
<td>50nm</td>
</tr>
<tr>
<td>Residue</td>
<td>7nm</td>
<td>8nm*</td>
</tr>
<tr>
<td>Residue - 3σ</td>
<td>3.9nm</td>
<td>0.6nm</td>
</tr>
<tr>
<td>Hole open yield</td>
<td>100%</td>
<td>100%</td>
</tr>
</tbody>
</table>

*Could be reduced by using thinner NL

Uniformity of the residue is improved using embedded NL
Defectivity: no more a blocking point for DSA integration

F. Delachat et. al., DSA Symposium 2016
DSA for contact patterning

Contact shrink

Fast material & process evaluation

Peanuts shape

DSA Pitch modulation by 193i pattern engineering

Elliptical template

Pitch density improvement by BCP natural period

Template by 193i
PS-b-PMMA BCP ($l_0 = 35$ or $46$nm)

Adapted from H. Yi, et al., Nano. Letters, 2015
Balancing BCP Thickness over Template Density in Graphoepitaxy

Full control of BCP self-assembly through pitch. All images are taken on the same processed wafer.
Summary

DSA has moved beyond the initial excitement of a new discovery.

DSA can easily meet resolution requirements down to N5.

Defectivity is still the main challenge, but the industry is making steady, order-of-magnitude progress each year.

DSA is on track to be adopted in manufacturing within two to five years.
DSA integration of lamellae-forming PS-b-PMMA ($L_0=38\text{nm}$)

CMOS architecture evolution

**Targeted application in Leti:** “tri-gate nanowires”

**Planar transistor**
- 2D channel

**Trigate Nanowire**
- 3D channel

**Stacked nanowires**
- Multi 3D channels

1. 193-d L/S pattern
2. PS homopolymer grafting
3. PS-b-PMMA coating and self-assembly (250°C for 5min)

Periodic like variations of residual PS bottom layer

UV expo to selectively tune surface affinity

UV-assisted graphoepitaxy process: neutral bottom / PMMA sidewall affinity

Post DSA: CDU = 1.4nm / LWR = 2.2nm / LER = 3.8nm

A. Fully neutral patterns induce "ladder" organization
B. Intermediary modification, neutrality partially disappear on patterns' top.
C. Optimal modification, sidewalls shifted from neutral to PMMA affine.
UV expo improve patterns after etching

<table>
<thead>
<tr>
<th>Standard process</th>
<th>UV assisted process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry PMMA removal</td>
<td>Bridge at bottom</td>
</tr>
<tr>
<td>SiO2 etching</td>
<td></td>
</tr>
<tr>
<td>Strip/litho/etch cut</td>
<td></td>
</tr>
<tr>
<td>Si etching</td>
<td></td>
</tr>
</tbody>
</table>

UV exposure avoid pattern collapse and reduce bridging defects

G.Claveau et al. SPIE 2017, 10144-36,
Process overview

Photo layer: Trilayer
Hard mask: SiO2
SiN
SOI wafer: Si
SiO2
Si substrate

CUT demonstrated on Si nanowire level
Guiding Pattern vs DSA Line Edge Roughness Characterization

- LER is transferred from guiding pattern to the 1st DSA line
- Lines 2 and 3 roughness is reduced due to the anneal process
Guiding Pattern vs DSA LER Characterization with PSD

- Low roughness frequencies are transferred from the guiding patterns to the DSA pattern
- LER increase for edge 2 and 7, it is significantly reduced for 3 & 6
- After PMMA removal the anneal process reduces DSA roughness
Summary

UV-assisted graphoepitaxy approach for a precise control of template affinity.

300mm compatible silicon nanowires patterning with DSA process (litho, etch, cut).

Next:
Electrical performances meas. and comparison to double patterning.

DSA patterning for stacked nanowire devices.

Investigation of BCPs with lower resolution.
300mm Chemoepitaxy Process

1. Brush grafting to the SiArc/SOC substrate
2. E-beam Lithography on PTR
3. O₂ modification
4. Resist stripping
5. BCP spin-coating

DMF: Density multiplication factor
SEM images w/a removing PMMA

PS-b-PMMA Nanostrength® EO L28 blends, from Arkema

Blends enable to achieve higher multiplication factors L/S patterns with low defectivity.

L. Evangelio Araujo et al. Proc of SPIE 2017, 10146-71
Ebeam cut on DSA patterning

E-beam exposure induces selective PMMA removal

DSA only:

E-beam cut on DSA:

20nm x 60nm CUT

1. 193d SIARC/SOC
   L/S pattern
2. Surface layer:
   PS grafting
3. PS-b-PMMA coating
   and self-assembly
4. E-beam lithography
5. Selective development

G. Claveau et al., DSA Symposium 2016
DSA technology: from PS-\textit{b}-PMMA to High-\(\chi\)

**Nodes**

- **L_0** (nm)
  - 38
  - 30
  - 24
  - 18

**FIN Pitch**

- 48nm (N14)
- 36nm (N10)
- 30nm (N7)
- 24nm (N5)
- - (N3)

**Materials**

- [193i + SADP]
- [193i + SAQP]
- [193i + SAOP] or [EUV]

**DSA of High-\(\chi\) materials:** a real competitive patterning option for sub-7nm nodes
### Silicon free High-χ

<table>
<thead>
<tr>
<th></th>
<th>Standard PS-(b)-PMMA</th>
<th>Organic High-χ</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_0) (nm)</td>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td><strong>Fingerprint performances</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD (nm) L/S</td>
<td>12.0 / 9.0</td>
<td>9.6 / 8.2</td>
</tr>
<tr>
<td>LWR (nm) L/S</td>
<td>2.7 / 1.6</td>
<td>1.5 / 1.1</td>
</tr>
<tr>
<td><strong>Graphoepitaxy performances</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD (nm) L/S</td>
<td>11.8 / 9.4</td>
<td>11.5 / 6.0</td>
</tr>
<tr>
<td>LWR (nm) L/S</td>
<td>2.0 / 1.1</td>
<td>2.0 / 1.22</td>
</tr>
</tbody>
</table>

Organic High-χ implemented on 300mm pilot line, compatible with the standard PS-\(b\)-PMMA process.
Silicon containing high $\chi$: PS-\textit{b}-PDMSB

Detailed lithographic performances under investigation on large areas. Next step: process transfer from samples to the track.
Bio sourced High $\chi$

GISAXS

PDMS-$b$-AcXGO

Inorganic block

m, n = 0 or 1 and s = 43 or 64

Organic block

L0 = 14nm

CD < 8nm

Djamila Ouhab PhD
A large panel of materials and process flows available.
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Celia Nicolet
Remi Letiec
Antoine Legrain
Francesc Perez Murano
Kaumba Sakavuyi
Harold Stokes
Marc Zelsmann
YOU ARE WARMLY INVITED TO ATTEND

We hope you will help us do this by sponsoring the 4th International Symposium on DSA.

On the behalf of program chairs: Tsukasa Azuma, Geert Vandenberghe, Raluca Tiron, and Joe Kline

http://dsasymp.org/
INTEGRATION CONCERNS

POTENTIAL SHOWSTOPPER FOR DSA

- Dense
- Isolated
- Mat edge

All images are taken on the same wafer

BCP performances depends on guiding patterns density
Defectivity over template density induced by BCP film thickness variation
A NEW METHOD TO CONTROL BCP FILM THICKNESS OVER PITCH

patent pending

1/ Guiding pattern

2/ Gap filling with BCP

3/ BCP bake

4/ Etch back

5/ Etching transfer

P. Pimenta-Barros et al, Proc. of SPIE 2015, 9428-12
Old process filling guiding patterns directly with final film thickness

New process: using DSA planarization