Plasma etch and deposition solutions for SiC and GaN devices

Oxford Instruments Plasma Technology
TechLounge, Semicon Europa 2018
Oxford Instruments Plasma Technology

We take cutting edge research technology to production

Design leading plasma processing etch and deposition solutions for Lab to Fab

Lab
✓ Leading technology enabling new applications
✓ Maximised device performance

End market segments

- Academic 51%
- Commercial 49%

Fab
✓ High reliability on high end platforms
✓ Low Cost of ownership with maximised yield
✓ Responsive service

• Unrivalled plasma processing knowledge
• Install base > 3000
Discrete
GaN SiC material for RF and Power devices. Failure analysis (Metal, polymer, Si)

Sensors
IR sensors, VOx, Si, Quartz MEMS

Optoelectronics
Laser and LED based on InP, GaN, GaAs

Nanotechnology
Graphene, MoS₂, WS₂...

Biomedicals
Micro fluidics coating and new materials
Automotive – Power conversion

• Adoption of wide band gap power conversion devices with improved efficiency over silicon.
• OIPT solutions developed to support fabrication of HEMTs, Inverter, MOSFET, IGBT, rectifier, filters…
• Processing solutions tailored to Compound semiconductor requirements with patented clamping technology and optimised chemistry.

“Smart Green World for a more sustainable energy and better device energy efficiency”
GaN RF Device Solutions
Front end processing solution for e mode GaN HEMT

Our offering

✓ Gate recess and passivation on same platform using ALE and ALD.
✓ Control of material quality at gate interface.
✓ Fast Via process selective to GaN
Low damage etch solution for very thin layers

Atomic Layer Etching

• Single atomic layers etching
• Precise control of etching depth
• Extremely low damage
• Plasma Technology large experience in providing ALD equipments makes us a supplier of choice for ALE.
• PlasmaPro 100 customized for ALE processing
• Patent application EP16187143
ALE of AlGaN and GaN

- Cyclical ALE process enables precise control and low damage
- Plasma can be on throughout cycle (or be switched on/off)

![Cyclical ALE process diagram]

- Oxidising dose gas, e.g. N$_2$O for controlled oxidation
- Oxidation is self-limiting
- Cl$_2$ etch gas removes the oxidised layer

AlGaN Oxidised surface

1. Dose
2. Purge
3. Etch
4. Pump

Oxidised surface

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AlGaN/GaN ALE results: Ar/Cl₂

- Etch rate 1.5-3 Å/cycle
  - up to 18 Å/min
- Uniformity <±5% over 200mm
- Added roughness <<1nm
  - AFM data indicates a smoothing effect

AFM data courtesy of Paolo Abrami in Collaboration with Bristol University
• Specially configured for ALE:
  • Fast recipe control down to 10ms
  • ALD-style gas dose delivery using “ALD valves” with 10ms open-close response
  • Ability to operate as a standard etch tool or in fast low power ALE mode. Mode selection via software recipe control

• PlasmaPro100 Cobra300
ALD of gate dielectric for low $D_{it}$

- Key application: ALD of high-quality $\text{Al}_2\text{O}_3$ to control GaN interface
- Effective passivation and isolation through excellent electrical properties
- Optimized for sensitive interfaces to minimize interface states and border traps

ALD materials of interest for GaN passivation and dielectric deposition:
- $\text{Al}_2\text{O}_3$
- $\text{AlN}, \text{SiN}_x, \text{GaN}$
- $\text{HfO}_2, \text{SiO}_2$
Nitride interlayer as pretreatment for HEMTs

- Use plasma treatments to form high-quality nitride interlayer.

Strong reduction of Ga-O bonds

Electrical characteristics:
- small sub-threshold swing 64 mV/dec
- a small hysteresis of 0.09 V
- low interface trap density of $1-6 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$.

Yang et al., IEEE Electron Device Lett. 34, 1497 (2013)
Epitaxial AlN for GaN thin-film transistor

- Epitaxial growth of ALD AlN using TMA and H$_2$/N$_2$ plasma at 300 °C. Followed by ALD Al$_2$O$_3$ gate dielectric.
- TFTs with good gate control with low subthreshold swing (∼85 mV/decade) and low-field mobility (∼27 cm$^2$/V·s).

SiC Power Device Solutions
Our offering

- Controlled roughness for improved leakage current
- Excellent profile from vertical to sloped with no micro-trenching for better device breakdown
- Conformal coatings with exceptional fill capability
Challenges in SiC Trench Etch

- **Challenges**
  - Reducing Surface Roughness
    - Improve leakage current
  - Reducing Micro-trenching
    - Improve Device Breakdown
  - Sidewall Angle control
    - From vertical to sloped profile
SiO$_2$ Hard Mask and SiC Trench Etch

- **Process Results**
  - **No Micro Trench**
  - **Etch Rate** > 700 nm/min
  - **Sel SiC:SiO$_2$** > 2.1:1
  - **Profile** ~ 86°
  - **Uniformity** > +/- 2.2%
  - Extremely smooth
RF and Power Semiconductor Summary

- **Market leading solutions** for high volume manufacturing
- Process and equipment designed to provide maximum yield up to 150mm wafer size at **market leading cost of Ownership**
- **Global Support infrastructure** to satisfy production customer's requirements