More than Moore with engineered substrates

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Agenda

1. Semiconductor roadmap needs engineered substrates
2. Engineered substrates enable high growth markets and applications
3. Industry-wide collaboration required to develop new standards
Soitec at a glance

DESIGNER & MANUFACTURER OF INNOVATIVE SEMICONDUCTOR MATERIALS

1. Largest manufacturer of engineered substrates
   LEADER

2. Unique technologies
   SMART CUT™, SMART STACKING

3. High-growth markets
   SMARTPHONES, AUTOMOTIVE, CLOUD & INFRASTRUCTURE, IOT

4. Wafer fabs (150, 200 & 300 mm)
   FRANCE, BELGIUM, SINGAPORE, CHINA*

5. Employees Worldwide
   GLOBAL PRESENCE

We design and deliver innovative substrates & solutions to enable our customers’ products shaping everyday life.

*Partnership with Shanghai Simgui Technology Co. Ltd. (Simgui)
Delivering the foundation of electronic circuits
Pushing boundaries to accelerate innovation

Using more MATERIALS

Applying unique PROCESSES

Crystal on crystal (lattice compatible)
Crystal on crystal (lattice compatible)
Crystal on crystal (not lattice compatible)
Crystal on amorphous

Smart-Cut™
Thin & highly uniform layers

To enable new APPLICATIONS

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Enabling new applications
Enabling new applications … by providing right solutions for PPAC
More than Moore – essential path to enable PPAC roadmap

More than Moore: diversification

Analog/RF
Passives
HV Power
Sensors
Actuators
Biochips

More Moore: miniaturization

Baseline CMOS: CPU, Memory, Logic

Beyond CMOS

Combining SoC and SiP: higher value systems

2.5D, 3D
More than Moore – essential path to enable PPAC roadmap and deliver on key drivers for markets and applications

Energy efficiency
Form factor
Reliability and security
Platform roadmap
Communication
Function integration
Cost for mass adoption
Better sensors and displays

Innovative device architectures
Material Innovation
Disruptive technologies
New Circuit design techniques

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Material innovation – engineered substrates

**ENGINEERED SUBSTRATES**

Applicable to silicon and non-silicon materials

**New materials**

- Device Layer: Silicon, Strained Silicon, Germanium, III-V...
- Functional/insulator layer: SiO2, ONO...
- Handle Substrate: CZ Silicon, High-resistivity Si, Sapphire, Glass, SiC

**New segments**

**New structures (2.5D / 3D)**

**Improved processes**

**SMART CUT™**

**SMART Stacking™**

**EPITAXY**

**COMPOUND SEMI.**

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Silicon and non-silicon engineered substrates in 150-, 200- & 300-mm
Few examples of Engineered substrates

- RF-SOI for 4G / 5G communication
- Silicon-Photonics for Data Centers and 5G
- Piezoelectric-On-Insulator (POI) for 5G RF filters
- FD-SOI for next generation MOU platform
- SmartCut™ SiC for EV
RF-SOI: an industry standard for Front-End Module (FEM)

Value proposition

- RF-SOI is present in 100% of smartphones
- RF-SOI is a standard for RF FEM components (antenna tuners, switches, LNAs, PAs)
- RF-SOI is a unique platform for FEM integration
- RF-SOI provides inherent isolation and signal integrity for LTE and 5G
- Best in class performance per cost

Product roadmap covering a complete 4G/5G FEM RF

-100dBm  eSI100T
-90dBm   eSI90
-80dBm   eSI80
-70dBm   IFEM-SOI
-60dBm   mmW-SOI
           HR-SOI
Photonics-SOI – path for 100GB/s and above connectivity

SOI SUBSTRATE

CMOS PROCESSING

OPTICAL WAVEGUIDE

Integration platform for complex optical function using CMOS fab

High speed modulation compliant

Low loss wave guide

Scalable solution for:
- integration
- performance
- cost

Silicon photonics growth drivers:
- Data center traffic
- Optical transceivers for data rate >= 100G/s
- Optical chip-to-chip interconnect
- Quantum computing

SOI defines the waveguides in the vertical dimension
SOI is directly linked to final optical performance
Piezo-On-Insulator (POI) – disruptive path to 5G RF Filters

**Product description**

POI:
Thin piezoelectric layer on oxide on high resistivity silicon

For the manufacture of high performance surface acoustic wave (SAW) filters

**Value proposition**

<table>
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<tr>
<th>Requirements</th>
<th>Impact</th>
<th>Soitec value proposition with POI</th>
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<tr>
<td>Data rates up to 20Gb/s</td>
<td>High frequencies</td>
<td>High quality factor</td>
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<td></td>
<td>Larger bandwidth</td>
<td>High temperature stability</td>
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<td></td>
<td>Band density</td>
<td>Low loss filters</td>
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<td>Battery life</td>
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<td>Up to 100 filters per smartphones</td>
<td>Component density</td>
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<td>Power dissipation</td>
<td>Better thermal conductivity</td>
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<td>Fast ramp to volume</td>
<td>Quick product design</td>
<td>Design acceleration with frec</td>
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<td>High volume manufacturing</td>
<td>Dedicated fab for POI</td>
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<td>HVM demonstrated on RF-SOI</td>
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FD-SOI – a perfect platform for AIOT with 5G connectivity

Standard MCU

NVM  CPU  Interfaces

>40nm

Intelligent MCU

Wireless  Security  AI

eNVM  CPU  Interfaces

Driver = power / bit / range

Driver = #Flops/W (energy efficiency)

Activity recognition
Sensor analysis
Audio recognition
Object detection
Computer vision

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FDSOI & Body Bias: Energy Efficiency without limits - key for AIOT and 5G connectivity

Adaptative Body Bias
Nwell, PWell regulation

Digital Area

Static FBB

6X LESS LEAKAGE

7X MORE PERFORMANCE

Courtesy of Dolphin Design – October 2019

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Silicon carbide (SiC) – big value and opportunity but only for right solution

SiC vs. Silicon
Performance improvement and size reduction in inverter

From Si-IGBT based module to SiC MOSFET based module:
- miniaturization: 30%
- weight Reduction: 40%
- high power density: >1.5times

Extra 60 miles of cruising range!

Source: Rohm

Key challenges to enable mass adoption
- SiC wafer capacity
- Substrate and device yield
- Performance and integration roadmap
- Lower wafer cost and capex
SmartCut™ based SiC substrates will trigger mass adoption of SiC

**Product description**

- **Existing substrate technology (epi-ready SiC)**
- **New substrate technology (epi-ready SiC)**

**Expected advantages**

- Higher yield versus SiC bulk
- Better performance
- Lower wafer cost and capex
- Sampling 150-mm for device development & developing 200-mm
Industry-wide collaboration required to develop new standards
Take-aways

1. Material innovation is key in securing “More Than Moore” roadmap

2. Soitec’s SOI engineered substrates have become industry standards across key markets and applications

3. Engineered substrates go beyond SOI products integrating:
   - New materials
   - New circuit design techniques
   - Innovative device architectures

4. Nothing will be possible without extensive collaborations across eco-system
   - unique path to disruptive solutions (from materials to system)
   - fastest way to reach the market adoption
Thank you

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