SiGe BiCMOS and Photonic technologies for high frequency and communication applications

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Outline

• Introduction & Motivation
• SiGe HBT device developments for high RF performance
  – Optimization towards 700 GHz $f_{\text{MAX}}$
• Electronic-Photonic-Integrated-Circuit (EPIC) SiGe-BiCMOS
  – Integrated components, transmitter & receiver circuits
• Summary
THz SiGe HBT and BiCMOS
Motivation

• High-speed SiGe HBTs used today for:
  – Automotive radar @ 24 GHz, 77 GHz and 120 GHz for transportation
  – High data rate optical and wireless links …

• Cut-off frequencies ($f_T$, $f_{max}$) typically 3-10X larger than operating frequency
  – Larger design margins, lower noise, higher gain, better linearity
  – Lower power consumption
Motivation (cont)

• Further enhanced RF performance needed for potential new applications:
  – Back-haul for 5G mobile comm. (optical or wireless)
  – Short-range wireless links for high data rates
  – mm and sub-mm wave imaging and sensing in medicine, industry, and science
  – High-resolution sensors for robotics

• SiGe BiCMOS targets frequencies and data rates which are out of reach for state-of-the-art CMOS
European Projects on SiGe HBTs

• Enhancement of HBT performance and exploration of new application areas addressed
• DOTFIVE (2008-2011)
  – Demonstration of HBTs with 500 GHz $f_{\text{MAX}}$
• DOTSEVEN (2012-2016)
  – Demonstration of HBTs with 700 GHz $f_{\text{MAX}}$
• TARANTO (started 2017)
  – BiCMOS platforms with 600 GHz $f_{\text{MAX}}$ targeting:
    • Advanced automotive radar systems
    • Infrastructure for 5G wireless and 400 Gb/s optical links
HBT Optimization & Process Modifications

• Starting point: IHP’s 130nm BiCMOS “SG13G2”
  – Highly-doped collector isolated by STI
  – Elevated extrinsic base
• Exploration of HBT performance limits irrespective of CMOS process constraints

Starting Point SG13G2

Final Status (D7)

- Narrower Silicide Blocking Spacers
- External Base Formation
- Reduced Width of Emitter & Emitter-Base Spacer
- Nickel Silicide
- Millisecond Flash Annealing & Low-Temperature Backend
- Scaled Emitter-Poly Width & Collector Window
- SiGe Base Profile & Adjacent Low-Doped Emitter & Collector Region

[Heinemann, IEDM 2016]
Enhancement of $f_T$ and $f_{\text{MAX}}$

- Results of the DOT5 and DOT7 projects compared to IHPs 1st generation 130nm BiCMOS
SiGe-HBT & BiCMOS performance evolution

- **Successfully finished**
  - Simultaneously $f_T > 400$ GHz and $f_{\text{max}} \approx 700$ GHz for discrete HBT achieved
  - Advanced HBT module (~0.5 THz) integrated into 0.13µm BiCMOS process of IFX

**Demonstrator:**
- 240 GHz RF chip-set + package (EuMW '16)
- 240 GHz radar transceiver + package + circular polarization (EuMC '15)
- 550 GHz full Si CT scanner (IRMMW-THz '16)
122GHz Radar as SiP and SoC (“SG13G2” == 0.5 THz – SiGe-BiCMOS)

- **System Requirements**
  - Frequency: 122-123 GHz ISM
  - Pout: 0 dBm
  - GT = GR: 10 dBi
  - NF: 12 dB
  - BW: 1 GHz

- **Modulation**: CW/FMCW
- **Distance**: up to 5 meters

⇒ On-chip integrated antenna by LBE process
Photonic-SiGe-BiCMOS (EPIC)
Silicon photonic transceivers

- Different market segments of optical/photonic area (telecom, automotive …)
- Requirements for continuous growth in bandwidth and IP traffic in optical networks, Long Haul and Metro applications
- **Goal:** Join basic components of e/o Transceiver (modulator, driver, amplifier, photo-detector,..)

### Major application areas for SiPh transceivers

- **Metro**
- **Data center**
Transceivers are a multi-chip assembly

Classic co-packaging assembly:
- High-speed DSP
- Serial/Parallel CDR
- High-speed DAC/ADC

Co-packaging assembly with ePIC:
- High-speed DSP
- Serial/parallel

Components:
- Tuning
- Driver IC
- TIA IC
- Control
- Fiber/laser
- ePIC
- Fiber/laser

ePIC = electronic Photonic IC
Major silicon ePIC approaches/technologies (select.)

**Hybrid / Co-packaging**

- Copper pillar technology

  G. Denoyer et al.; JLT 2015

**Monolithic FEOL / CMOS Photonics**

- Photonic SOI CMOS
- Zero-change Photonic CMOS
- ....

  JS Orcutt et al.; OFC 2016

**Monolithic FEOL / Photonic BiCMOS**

- Joint: CMOS + SiGe HBT + PIC

  IHP work

**FEOL = Front End of Line**
Photonic BiCMOS 1st generation development goals

- 0.25µm RF-CMOS
  - 5 ML / MIM
- SiGe HBTs
- SG25H4 BiCMOS baseline
  - 170GHz $f_T$
  - 200GHz $f_{max}$
  - 1.9V $BV_{CEO}$

- Ge-PDs (high bandwidth, resp.)
- MZI modulator
- “130nm node” passives

State-of-the-art Si-photonics

Strict modularity of photonic integration

- Re-use of parent BiCMOS devices (models)
- No BiCMOS yield degradation
- Re-use of DigLib
Central for EPIC– process integration

- Shared wafer
- Mixed Substrate:
  - Localized SOI areas for optical structure
  - Bulk like substrate for BiCMOS structures
- Common backend
- Modulized process flow
PIC- and EPIC-technology at IHP

1. Mature 0.25µm-BiCMOS Technology available (SG25H4)

2. Development of PIC-process (Photonic Integrated Circuit) based on established 0.25µm-BiCMOS Technology (SG25_PIC)

3. Integration of PIC in BiCMOS → EPIC (Electronic Photonic Integrated Circuit) (SG25H_EPIC)
   - More than 30 Masks
   - More than 700 process steps
EPIC Transmitters
Silicon cross section structuring

- 3 etching depths available: 220nm, 120nm, 70nm
  - Vertical structuring is limited
  - Freedom in horizontal structuring
- Dopings: p, n, p+, n+

Diagrams:
- Grating structures
- Rib waveguide
- Wire waveguide
Transmitters differ in phase shifter structure

- Depletion type
- Injection type
Mach-Zehnder modulator – segmentation

Traveling wave electrode:
• Significant RF loss on the line
• Limited bandwidth and extinction ratio
• Velocity mismatch between optical and electrical waves

Segmented MZM:
• Modulator divided into lumped segments
• Constant voltage along the phase shifter \(\rightarrow\) high ER
• Bandwidth expected to be less dependent on length \(\rightarrow\) longer phase shifters can be driven effectively with low driving voltage
Single MZM with linear driver

- 6 mm phase shifter divided into 16 segments
- Total fiber-to-fiber loss equal to 17 dB (5 dB from the phase shifter)
- Power dissipation equal to 2W or 71 pJ/bit at 28 Gb/s
- EO bandwidth 18GHz

D. Petousi et al, Monolithic Photonic BiCMOS Sub-System Comprising Broadband Linear Driver and Modulator Showing 13 dB ER at 28 Gb/s, CLEO, 2016
MZM + driver with integrated DAC

Concept:

- Utilizing the segmentation of the modulator
- Integrated DAC resolution is limited due to layout and area constraints.
- With digital inputs, the driver is implemented as switching amplifier reducing power dissipation
- NO EXTERNAL DAC.

Integrated Germanium photo diode

Performance
- $f_{3db} > 65$GHz@-2V
- R > 0.9A/W
- $I_{dark} < 100$nA@-1V

$V_{bias} = 0V, \lambda = 1550$nm
mean = 42GHz ($\sigma = 2$GHz)

S. Lischke et al. *Optics Express* 23 (21), 2015
Jeong-Min Lee et al, *Photodetection Frequency Response Characterization for High-Speed Ge-PD on Si with an Equivalent Circuit*, WA2-78, *OECC 2016*
GePD: Benchmark – Responsivity, e/o BW and dark current

- Fully integrated Ge PD in BiCMOS exceed performance level of discrete PD
- Enabler for high efficient Rx EPIC designs
Recent results – linear SP receiver

Extended BW (36GHz)

Up to 56Gbps NRZ OOK

32 Gbps

40 Gbps

48 Gbps

56 Gbps

Reference PD

28Gbd PAM4

IHP Rx

M. Kroh et al, Monolithic Photonic-Electronic Linear Direct Detection Receiver for 56Gbps OOK, ECOC 2016
Photonic BiCMOS evolution

Demonstrators: **monolithically integrated O/E RECEIVERS**

- **2014**
  - 25 Gbps
  - [Knoll et al., OFC 2014]

- **2015**
  - 40 Gbps
  - [Awny et al., MWCL 2015]

- **2016**
  - 56 Gbps
  - [ECOC2016 & ESSCIRC2016]
Photonic BiCMOS evolution

Demonstrators: monolithically integrated E/O MODULATORS

2013

10 Gbps [Zimmermann et al., ECOC 2013]

2016

32 Gbps [Petousi et al., PTL 2016]
Summary

• Record values of $f_T=505\,\text{GHz}$, $f_{\text{MAX}}=720\,\text{GHz}$ and $\tau_{\text{RO}}=1.34\,\text{ps}$ demonstrated in an experimental SiGe HBT process
  – Room for further improvements by lateral scaling

• EPIC technology developments show potential for beyond 100Gbit/s optical interfaces

• Ongoing challenging task of integrating these HBTs and Photonic modules in a BiCMOS platform
Acknowledgment

• IHP colleagues H. Rücker, B. Heinemann, D. Kissinger, H. Ng., L. Zimmermann, D. Knoll, S. Lischke, D. Petousi & M. Kroh

• IHP clean room staff

• Project partners and funding sources EU (H2020) & BMBF
Thank you for your attention!