Disruptive NVM technologies in Russia

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Content

- Disruptive NVM technologies
- CNE is a new-generation NVM fab
- MRAM technology development
- ReRAM (CBRAM) technology acquisition
Emerging NVM overview

MRAM
➢ Non-volatile memory based on magnetic storage elements, not on electric charge or current flow like standard memory
➢ Advantages
  ➢ Very high write speed
  ➢ High endurance (up to unlimited)
  ➢ STT MRAM: low power consumption (100x better than MRAM)
  ➢ STT MRAM: perfect scalability potential (below 20nm) / compatible with standard CMOS
➢ Current status:
  ➢ Density: 1Gb (Everspin)
  ➢ Node: 28 nm (Avalanche/UMC) / 300mm wafers

RRAM
➢ Resistive RAM consists of the localized, filamentary nature of a conductive path formed in an insulating material separating two electrodes structure, corresponding to the on-, low-resistance state
➢ Advantages
  ➢ Standard CMOS compatibility: low cost
  ➢ High speed compared to flash
  ➢ Low programming voltage (<3V) and low current (sub μA) => low power consumption
  ➢ High scalability: 4F2 cell => scaling up to 10nm
  ➢ 3D array capability
➢ Current status:
  ➢ Density: 4Mb (Fujitsu)
  ➢ Node: 40 nm (Crossbar/SMIC)

PCM
➢ Phase-change memory – is a type of non-volatile computer memory which utilizes unique behavior of chalcogenide glass material
➢ Advantages
  ➢ Good scalability: potentially below 10nm for stand-alone
  ➢ Small cell size: 6-12F2 for S/A and 18F2 for embedded SoC
  ➢ Cost competitive (few masks)
➢ Current status:
  ➢ Density: 128Gb (Intel)
  ➢ Node: 20nm (Intel)
Emerging NVM opportunity

New memory technologies: new physical principles versus old challenges

**NAND flash**
- Scalability: multilayers (over 128) process uniformity, precise etch, sophisticated controller
- Endurance: P/E cycles wear
- Power consumption
- Latency

**DRAM**
- Scalability: taller capacitor, interferences => reliability
- Volatility

Advanced memories benchmark

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Typical memory technology</th>
<th>New memory technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SRAM</td>
<td>DRAM</td>
</tr>
<tr>
<td>Non-volatility</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Cell size (F²)</td>
<td>50-120</td>
<td>6-10</td>
</tr>
<tr>
<td>Read time (ns)</td>
<td>≤2</td>
<td>30</td>
</tr>
<tr>
<td>Write time (ns)</td>
<td>≤2</td>
<td>50</td>
</tr>
<tr>
<td>Write power</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Endurance (cycles)</td>
<td>10¹⁶</td>
<td>10¹⁶</td>
</tr>
<tr>
<td>Future scalability</td>
<td>Good</td>
<td>Limited</td>
</tr>
</tbody>
</table>
Emerging NVM in the market

Market adoption challenge

- Limited density, technology node: still under the SCM demand
- Process&materials complicity: delays in Everspin, Samsung, Hynix/Toshiba, Micron programs
- Improved scalability for NAND/DRAM technologies
- Low focus of leading foundries - TSMC, Samsung, GF

Step forward

- Total memory market is expected to reach 100B$ in Y2022
- Major trend towards power consumption
- Smaller nodes for emerging NVMs will make SCM achievable
- Major foundries will enter the market
CNE is a pure-play 300 mm BEOL Foundry with state of the art equipment, advanced process technologies and capabilities.

2011
Crocus Technology and Rusnano created JV – CNE

2013
Industrial manufacturing for magnetic layers at CNE

2015
- BEOL cycle implementation at CNE
- Completion of 300mm fab

2016
- Start of TMR pilot production and foundry prototyping
  - ISO 9001:2008 certified

2017
- Proprietary MRAM technology – start of development
  - Qualification of TMR and Bio-chemistry-sensors

2018
- Created Ecosystem for Test and Packaging
  - Started Adesto CBRAM technology transfer
  - ISO 9001:2015 certified
CNE today

ABOUT CNE
• Pure-play BEOL foundry
• 90+ employees. International team of highly qualified engineers
• Export: 95%
• Quality management systems ISO 9001-2015

CLEANROOM
• 300mm wafer size
• Cleanroom Area  2 500 m²
• Classification ISO 4-7 (certified)

CAPACITY
• Capacity up to 4000 wafer per month (facility ready)
• Expansion area available
• Special magnetic capability (deposition, etch, annealing, metrology and test)
Main focus

EMERGING NON-VOLATILE MEMORY:

MRAM
RRAM

300mm MRAM

Embedded Memory
Magnetic Sensors.
High-Level Integration
Customized Projects

IC’s for RFID
Bio-Sensors

RFID

Embedded Memory
MRAM development challenge

STT MRAM principles
- Magnetic momentum data storage
- MTJ cell construction
- TMR and STT phenomena

CNE MRAM
- STT MRAM based on pMTJ cell
- Launched in Y2017 (Q1)
- Experienced R&D team collected
- Funded by CNE founders

Development challenge
- Material:
  - Low TMR: target level 200%
  - Anisotropy under high temperature: target $\Delta K_{eff} > 60$,
    Temperature +125°C
  - High write voltage: target $V_w$ must be ~0.4V (endurance)
- Process:
  - High $\sigma_R/R$: target level 1-3%
  - High errors rate: target 1ppm for Mbit range chip
  - Low TMR: process damage

Source: MARK LAPEDUS
STT MRAM development program

CNE test chip: Y2018

- Density: 4Kbit
- GF, 130 nm CMOS
- Test platform for MRAM development & test: variable switching time and Rmtj
- 150+ CMOS-driven 4 Kbit chip designs (MTJ size&integration)

Characterization

- Zero errors at 100 cycles
- Yield is reasonably high
- Bit yield definition:
  - Runs 10000 cycles
  - Survives (no breakdown)
  - 0 errors
  - Both switching directions for writes both 0 and 1
CNE MRAM future

300 mm wafer

Development area
➢ Technology node => 65nm
➢ Materials: TMR, Keff, temperature and V_w
➢ Process: bitwise yield, TMR

Short term: 2-3 years
Stage I: early commercialization
55/65nm node, 300mm wafers
Niche industrial applications

Medium term: 5 years
Stage II: MRAM foundry
40nm node, 300mm wafers
Industrial, IIoT, medical devices, RFID

Long term: TBD
Stage III: upgrade
14-28nm node, 300mm wafers
Storage, AI, Industrial, MCU, automotive, transportation

Product: eMRAM => MCU, SoC
Density: 1-2MB
Universal memory: NVM, RAM
High reliability
Low cost

Embedded and standalone
universal SCM
>1Gbit range

Density | 4 Mbit
Data retention | 25 years at RT
| 10 years at +105C
TMR | 100%
Write time | 100 ns
Read access time | 40 ns
Endurance | 1×10^{15}
Working temperature | -55...+85 °C

Memory test-chip

CNE CONFIDENTIAL
**CBRAM program overview**

**CBRAM® (Adesto) principles**
- Specific materials
- Convertible conductive bridge inside dielectric barrier
- Major resistance change: 0/1 cell

**CBRAM today**
- Ultra-low-power NVM
- High reliability
- Cost-efficient (1 mask adder)

**CNE CBRAM program**
- CNE fab configuration matching CBRAM process
- License Agreement with Adesto: Dec-2018
- Technology transfer completed: Dec-2019
- First product fab-out: Dec-2019
  - UHF RFID chip: 400 bit CBRAM NVM
  - NVM memory IP: 2Mbit CBRAM with SPI interface

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**CBRAM simulation, 2Mbit chip**

<table>
<thead>
<tr>
<th>Test</th>
<th>Condition</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gamma</td>
<td>200kGy (20M rad)</td>
<td>Passed</td>
</tr>
<tr>
<td>e-beam</td>
<td>200kGy (20M rad)</td>
<td>Passed</td>
</tr>
<tr>
<td>Heavy Ion</td>
<td>75 MeV·cm²/mg</td>
<td>Passed</td>
</tr>
<tr>
<td>High Temp (SMT)</td>
<td>10min @ 260°C</td>
<td>Passed</td>
</tr>
<tr>
<td>Magnetic fields</td>
<td>~10^3 Gauss</td>
<td>Passed</td>
</tr>
<tr>
<td>UV light</td>
<td>30min @ 12mW/cm²</td>
<td>Passed</td>
</tr>
</tbody>
</table>

**Test Condition Result**
- Gamma 200kGy (20M rad) Passed
- e-beam 200kGy (20M rad) Passed
- Heavy Ion 75 MeV·cm²/mg Passed
- High Temp (SMT) 10min @ 260°C Passed
- Magnetic fields ~10^3 Gauss Passed
- UV light 30min @ 12mW/cm² Passed

**CBRAM wafer**

<table>
<thead>
<tr>
<th>Density</th>
<th>2Mb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus</td>
<td>32bit</td>
</tr>
<tr>
<td>Power supply</td>
<td>0.9V; 3.3V</td>
</tr>
<tr>
<td>Read access</td>
<td>50 ns (32bit word)</td>
</tr>
<tr>
<td>Write time</td>
<td>25/100 us (32bit word)</td>
</tr>
<tr>
<td>Standby power</td>
<td>10uA</td>
</tr>
<tr>
<td>Dynamic read power</td>
<td>1.51mW (32bit word)</td>
</tr>
<tr>
<td>Dynamic write power</td>
<td>1.31mW (32bit word)</td>
</tr>
<tr>
<td>Endurance</td>
<td>100K cycles</td>
</tr>
<tr>
<td>Data retention</td>
<td>10 years (+105C)</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-40 ... +85C</td>
</tr>
</tbody>
</table>
THANK YOU