Advanced Transistor Evolution – Technologies for 5 nm and Beyond
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Abstract

For continuous CMOS logic scaling, new materials were introduced at the 65-nm technology node. This is considered as the end of traditional CMOS scaling by simple device dimension reduction. First, epitaxial stressors for strain engineering were introduced to obtain high carrier mobilities. Then, high-k metal gate (HKMG) followed at 45-nm node\(^1\). HKMG enabled scaling gate oxide thickness with reduced gate leakage current. From the 22-nm node, conventional planar transistors were no longer viable due to increased leakage by short channel effect (SCE). As a result, a new architecture, namely FinFET, was introduced\(^2\). FinFET suppresses SCE, enabling scaling down to the 7nm node\(^3\) and is expected to be utilized in 5-nm node devices.

Thus, material and architectural evolutions have been essential for advanced CMOS scaling. CMOS beyond 5-nm node will require further improved SCE by new transistor architecture. Horizontal gate-all-around (hGAA) FET is the most promising candidate because of superb gate control and flow similarity to FinFET\(^4\).

This paper describes CMOS evolution beyond 5-nm node by architectural changes and new material introductions including hGAA FET and conductive metal fill technology.

References


\(^3\) S.-Y. Wu et al., “A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027um2 High density 6-T SRAM cell for Mobile SoC Applications,” 2016 International Electron Devices Meeting, pp. 43-46.